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Power Supply for Piezoelectic Actuator

Thesis submitted for examination for the degree of Master of Science in Technology
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DIPLOMITYÖN
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Tässä työssä tutkittiin teholähderatkaisuja korkeajännitepietsotoimilaitteelle. Tavoitteena oli saada pietsotoimilaitteen jännite muuttumaan -200 voltista 1000 volttiin ajassa 0.5 ms. Pietsotoimilaitteen lataamiseen vaadittavan suuren virran takia työssä tutkittiin vain jännitettä nostavia topologioita. Lineaarisen teholähteen hyötysuhde olisi ollut ratkaisevasti huonompi.

Useita eri vaihtoehtoja simuloitiin SPICE -simulaatio-ohjelmistolla. Mittauksia varten suunniteltiin ja valmistettiin prototyypplaite, jotta voitiin tutkia teholähteen käyttäytymistä oikealla pietsokuormalla. Koska teholähteessä tehopuolijohdekomponenttien kytkentätaajuus valittiin välillä 50 - 100 kHz, oli piikarbidi MOSFET -kytkinten käyttö perusteltua.

Pietsopinoa ohjattiin avoimessa ja suljetussa silmukassa. Testeissä käytettiin kokosiltahakkuria, jonka ulostulo oli biasoitu. Näin kokosillan koko jännitealue saatiin hyödynnettyä pietsopinon ohjauksessa. Avoimen silmukan ohjauksessa pystyttiin ohjaamaan pietsopino -190 voltista 950 volttiin 0,6 ms (10% - 90%). Muutosten aikana huippuvirta oli 36 ampeeria.

Tavoitteet lähes täyttyivät jännitteiden ja muutosnopeuden osalta. Teholähteellä pystyttiin todentamaan, että pietsopinoa voidaan ohjata halutulla nopeudella.

Asiasanat:	pietso, toimilaite, piikarbiidi, ohjauselektroniikka
Kieli:	Englanti

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ABSTRACT OF
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This thesis presents a process of design, prototyping and testing of a power supply for high voltage piezoelectric actuator. And switch-mode converter topologies were examined while they provide better efficiency than their linear counter parts. The goal was to charge a piezoelectric stack from -200 V to 1000 V in under 0.5 ms.

The most interesting topologies were simulated with SPICE-simulation software to gain knowledge and reference. A prototype device was designed and build in order to examine topologies with actual a piezoelectric actuator. Since the switching frequency of the converter was 50 - 100 kHz, high speed SiC MOSFET modules were utilized.

The piezo stack was driven with open-loop and close-loop operation. A biased output full-bridge topology was used in actual measurements. In open-loop operation maximum output voltage difference of -190 to 950 V was reached while Rise and fall times (10 % - 90 %) was 0.6 ms. The peak current during transitions was 36 amperes.

The requirements were almost reached and the power supply proved that the piezo stack actuator can be driven with such a high speeds.

Keywords:	piezoelectic, actuator, SiC, Driver
Language:	English

Preword

First I would like to thank Prof. Jorma Kyyrä for guidance with the whole process. I also would like to thank Department of Engineering Design and Production stuff especially my instructor Jari Kostamo and research assistant Ville Klar for great support. I also like to thank Petri Kuosmanen, Thomas Widmaier and Jouni Pekkarinen. Then I wish to thank my ex-college Dai Trinh for technical support related to power supply in general. I also would like to thank my friends and family for support.

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Juha Vanhalakka

Used symbols and ja abbreviations

α_c	Carrier Phase-shift angle
ϵ	Dielectric constant
Λ	Reluctance
μ_0	Permeability of Vacoom
μ_r	Relatively Permeability
ϕ	Magnetic Flux
A	Area
B	Magnetic Flux Density
C	Capacitance
C_c	Coupling Capacitor
C_{cc}	Capacitance related to compliance constant of piezo
C_{ce}	Collector-Emitter Capacitance
C_{cg}	Collector-Gate Capacitance
C_{dg}	Drain-Gate Capacitance
C_{ds}	Drain-Source Capacitance
C_{ge}	Gate-Emiter Capacitance
C_{gs}	Gate-Source Capacitance
C_{iss}	Input Capacitance
C_o	Piezo Capacitance
C_{oss}	Output Capacitance
C_{rss}	Trans Conductance Capacitance
D	Duty Cycle
d	Distance
E_c	Capacitor Energy
f_a	Anti-resonance Frequency
f_r	Resonance Frequency
f_{sw}	Switching Frequency
H	Magnetic Field
i_C	Capacitor current

$i_{drv,p}$	Peak Driver Current
L	Inductance
L_m	Inductance related inertia of piezo
l_{tot}	Total displacement
N	Number of turns
Q_g	Total Gate Charge
$R_{ds(on)}$	Drain-Source resistance during on-state
R_f	Resistance related to friction of piezo
R_{jc}	Junction-to-Case thermal resistance
T_j	Junction Temperature
u_L	Inductance voltage
V_{bd}	Dielectric Breakdown Voltage
V_{cc}	Driver Supply Voltage
V_{ce}	Collector-Emitter Voltage
V_{dd}	Input Voltage
V_{ds}	Drain-Source Voltage
V_{ge}	Gate-Emiter Voltage
$V_{gs(th)}$	Threshold Gate Voltage
V_{gs}	Gate Voltage
V_O	Output Voltage
w	Width
AC	Alternative Current
ADC	Analog-to-Digital converter
BJT	Bipolar Junction Transistor
CHB	Cascaded H-bridge
CLA	Control Law Accelerator
DC	Direct Current
DMOS	Double-diffused Metal–Oxide–Semiconductor
EMC	Electro-Magnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCC	Flying Capacitor Converter
FET	Field Effect Transistor
FET	Field-Effect Transistor
FPGA	Field-Programmable Gate Array
FR4	Fiberglass Circuit Board Material
GaN	Gallium Nitride

GDT	Gate Drive Transformer
GND	Ground Reference
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction gate Field-Effect Transistor
LED	Light Emitting Diode
LSMC	Level-Shifted Multi-Carrier Modulation
MCU	Microcontroller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPC	Model Predictive Controller
MV	Medium Voltage
NPC	Neutral Point Clamped topology
NPT	Non-Punch Through
PC	Personal Computer
PCB	Printed Circuit Board
PSMC	Phase-Shifted Multi-Carrier Modulation
PT	Punch Through
PWM	Pulse Width Modulation
PZT	Lead Zirconate Titanate
RAM	Random Access Memory
Si	Silicon
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
THD	Total Harmonic Distortion
TIGBT	Trench Insulated Gate Bipolar Transistor
USB	Universal Serial Bus
WBG	Wid Band Gap

Contents

Chapter 1

Introduction

Piezoelectric materials have many applications in fields of engineering and medical solutions. New ways to utilize such materials are discovered frequently. Such materials have variety of properties, which are superior comparing to other technologies. Piezoelectric actuators can produce quick accurate movements which is preferable in many applications. However, the displacement that a single piezoelectric element can produce is quite minimal. So worth, there are many ways to amplify that small movement.

When examining the piezoelectric actuator as a load for power supply, it acts as capacitor. The capacitor must be charged and discharged quiet rapidly in order to achieve fast displacement. The charge energy can also be restored which makes piezo even more attractive. However, the mechanical structure of the piezo element is forming resonance circuit which makes it hard to increase the charge and discharger rates.

There are commercial high voltage piezo amplifiers available, however the output current is typically regulated under 10 A [22] [28] [24]. To achieve high fast rise and fall times, with piezo stack used in this experiment, the power supply must be able to source and sink over 30 A of current. Inspiration could be seek from switch mode audio power amplifiers and power inverters. These devices produce bipolar output waveforms with high power. Switch-mode power supply also provide superior efficiency compared to linear counterparts.

In this thesis Chapter 2 discusses about the theory behind the piezoelectric material and the electronics that is combined to build the power supply. Also previous research was studies. In Chapter 3 various simulations are made according to

discoveries in literature and previous knowledge. Chapter 4 explains the prototype platform witch was developed for testing purposes. Measurements that were done are represented in Chapter 5 and and conclusions are gathered in Chapter 6.

Chapter 2

Background

2.1 Piezo Transducer

The piezoelectricity phenomenon was discovered in 1880 by Jacques and Pierre Curie. The first materials were quartz and Rochelle salt, tourmaline and topaz. Later during 40s and 50s new materials such as ferroelectric ceramics barium titanate and lead zirconate titanate (PZT) become available. During the last few decades these materials have become more important due their potential as smart material. Piezoelectric materials can be used for both sensing and actuation while they convert mechanical energy to electrical energy and vice verse. Wide variety of engineering and medical applications have utilized piezoelectric materials for sensing inputs such as pressure, strain, vibration, rotation and sound. As an actuator piezoelectric materials are used in valves, switches, relays and robotics.[29, p. xi]

Piezoelectric materials are classified as noncentrosymmetric dielectric crystals. When an external electric field is applied to such a material, a asymmetric displacement of anions and cations will occur. This means that the material expands or compresses depending on the polarity of the external electical field which is stated as *indirect piezoelectic effect*. Utilizing this effect it is possible to construct piezoelectric actuators that have many advantages such as;

- low complex design
- considerable force generation
- quick response

- low input voltage.

An inverse phenomena also exist where an external pressure or strain applied to the piezo material will form positive or negative charge to opposite side faces creating electric field across the crystal. The effect is referred to *direct piezoelectic effect.* [29, p.10, 81]

[29, p. xi]

2.1.1 Stacked Actuators

In order to achieve longer strain for the piezo actuator, the piezoelectric elements have to be stacked. This way the the whole stack expands as follows:

$$\Delta l_{tot} = N\Delta l, \tag{2.1}$$

where Δl_{tot} is the total displacement and N is the number or elements forming the stack. Even for high voltages applied the strain of the piezoelectric material is about 0.1 - 0.2 %.

In a piezo stack the polarities of individual elements are faced toward each other so that polarity of every second element is the same. Electrodes are placed between every element are they are connected in parallel increasing capacitance of the stack. A structure of the stacked piezo actuator is presented in Figure 5.1. Usually some sort of mechanical amplification is applied to the piezo stack which magnifies the compression or expansion. However, these external mechanical structures cause increases response times, decreases force generated and also increases losses of the piezo stack.

[29, p.81-83]

2.1.2 Piezoelectric dynamics

A piezoelectric element can be modeled as a capacitor as follows:

$$C_o = \frac{\epsilon A}{d}, \tag{2.2}$$

where C_o is capacitance, ϵ is dielectric constant, A is area of the electodes and d is thickness of the piezo element. In parallel with electrical circuit there is mechanical

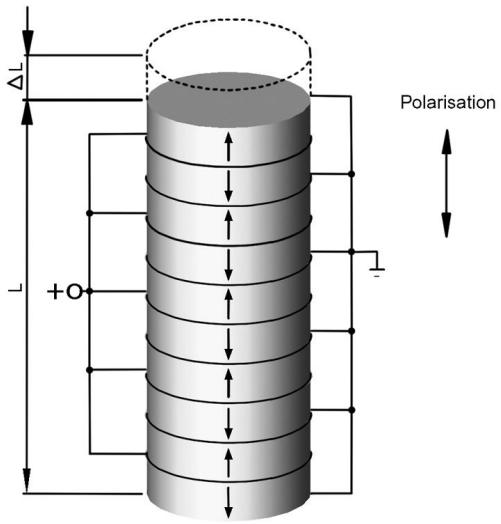

Figure 2.1: A piezoelectric stack. Individual elements are stacked and electrodes are placed in between so that the capacitances of the elements are in parallel. [23]

circuit consisting of mass (inertia), compliance constant and energy loss caused by friction. These components can be modeled as inductance L_m, capacitance C_{cc} and resistance R_f, respectively. The equivalent circuit is illustrated in Figure 2.2. Inductance L_m and capacitance C_{cc} form a series resonance circuit. The resonance frequency can be obtained by:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{C_{cc}L_m}}, \tag{2.3}$$

At resonance frequency impedance of the piezo element is zero if R_f is not taken into account. The low impedance is shown in transfer function as peak in amplitude.

These equivalent electrical reactances also form an antiresonance circuit which have opposite effect to the impedance and to the transfer function. The antiresonance frequency can be calculate as follows:

$$f_a = \frac{1}{2\pi}\sqrt{\frac{C_{cc}+C_o}{C_{cc}C_oL_m}}, \tag{2.4}$$

Resonance and antiresonance frequencies can be measured with a LCR -meter. These frequencies should be taken into account while designing the driving circuit.

Especially antiresonance phenomenon could be useful while designing the output circuit of the electronics.

[29, p.35-37]

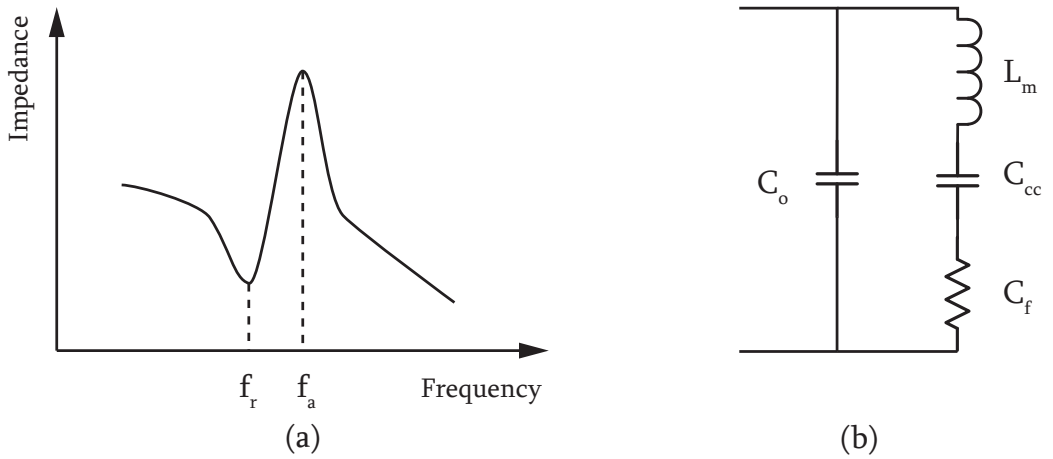

Figure 2.2: (a) piezo resonance f_r and antiresonance f_a frequencies, (b) piezo equivalent circuit. [29]

2.2 Driver Topologies

As stated in previous section, the piezo element can be treated as a capacitor and its displacement is a function of the voltage applied. The piezo actuator can be driven with analog driver circuit such as operational amplifier combined with linear power stage [3]. However, when the driver power increases also the losses in linear driver become insufferable due to relatively low efficiency of the driver. When output power is low and distortion must be low, a linear piezo electric driver is a good choice.

Utilizing switch mode-power electronics for driving piezoelectric actuators have become more and more popular. There are few advantages when using switch mode power supplies with piezoelectric actuator; the losses are quit low and energy stored to dielectric material can be recovered. Especially in automotive industry high efficiency is a key parameter. Also negative bias voltage, which is sometimes applied to utilize hysteresis of piezo elements, could be achieved easily with switch-mode

power electronics. As a result a wider extraction could be achieved with bipolar driving voltage. [12]

High voltage cannot be applied directly to the piezo actuator because it would draw enormous amount of current $i_c = C\frac{du}{dt}$ and break all components. Also the piezo could be damaged. Therefore, an external choke inductor is connected in series with the piezo actuator to limit the charging current. Inductor and capacitor form a series resonator circuit which has its resonance frequency similar to Eq. (2.2). As shown in Equation (2.2) the resonance frequency increases when the inductance decreases. Resonance frequency should not be reached because it causes unwanted oscillation. Capacitance of the piezo element is fixed meaning the only way to increase the bandwidth is to lower the inductance of the circuit. On the other hand, if the inductor is to small, the current ripple increases which worsen the Total Harmonic Distortion (THD) of the amplifier. Also, voltage difference applied to the inductor changes current as follows:

$$u_L = L\frac{di}{dt} \Rightarrow di = \frac{u_L dt}{L} \tag{2.5}$$

As the equation shows, current ripple can also be reduced by increasing the switching frequency. In literature as high as 500 kHz switching frequency has been used for the switch mode piezo drivers, meaning the choke inductance could have been kept quite minimal [6] [12]. However, the high switching frequency causes great demands for the other components such as MOSFET/IGBTs and their driver circuits. [6] If the Bode plot is examined, phase change at the resonance frequency from -90 ° to + 90 °. This means that at lower frequencies current is ahead voltage which means that the voltage of the piezo element rises after the current has been applied to it. Above the resonance frequency current start to develop after the voltage has been applied. While the switching frequency is above the resonance frequency, the circuit is said to be working on inductive region. [17, p.256]

2.2.1 Half-Bridge

Half bridge configuration has been used in variety of applications such as single phase inverter and D-class power amplifiers. Also in literature half bridge has been used to drive low voltage piezo actuators[6] [12]. Piezo as a load varies from other loads by absence of resistive parallel component attached to the system which consume energy. Piezo actuator is charged and discharged and no energy is lost in ideal situation. However the switching and conducting losses of valves and conduction losses of inductor choke are present in real situation.

There are two switching elements connected in series between the DC-rail and the load is connected to the center of the switch. This configuration is named as a leg and in multi phase inverters there is one leg for every phase. The switch pair in the leg cannot be conducting at the same time or shoot through occurs destroying the valves. The anti-parallel diodes provide current path during dead band region. Lower diode also conducts during charging and higher during discharging. The returning path of the load could be connected to negative rail or to the center of the two DC -condensers depending if negative output voltage is needed. In piezo application the negative voltage is usually needed.

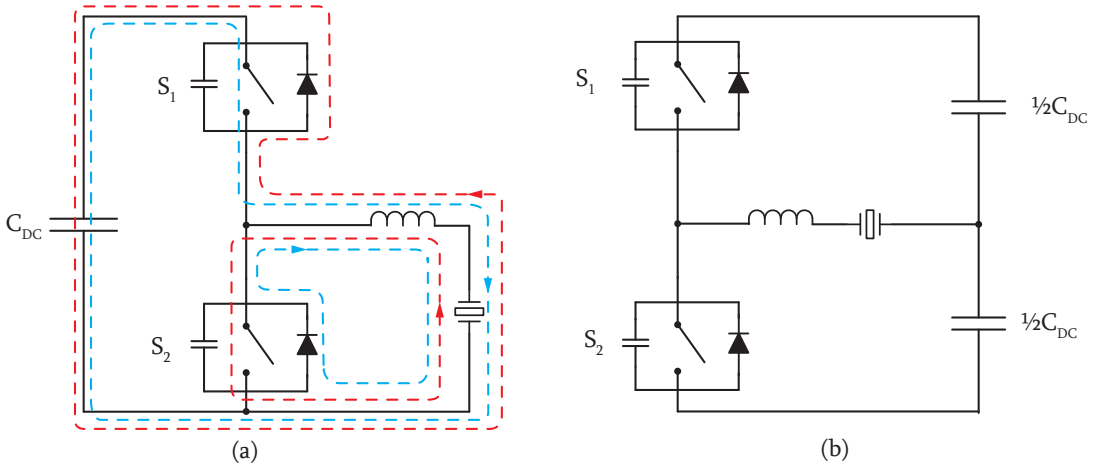

Figure 2.3: Half Bridge. (a) Positive voltage, (b) negative voltage possible.

If no negative voltage is needed, the half bridge configuration can be seen as two different DC-DC converts: buck and boost. While piezo is charged, upper valve is controlling the process and lower valve acts as freewheel diode. If MOSFET and synchronous rectification is used, also lower switch could be turned on to lower the conduction losses. In this mode the driver acts as buck converter. When the piezo is discharged, the lower switch is turned on and the inductor current start to rise. When the lower valve is turned off, the current starts to flow through higher diode. This mode can be seen as boost converter.

When negative voltage is needed, the other end of the piezo element is attached at the mid point of the DC-rail. If the capacitances are equal, the voltage should be at the middle of the zero and Vdd. However, the midpoint can drift and parallel high impedance resistors could be used to balance the voltages.

Controlling of the half bridge is usually done by PWM-modulation where triangle or sawtooth waveforms are compared with reference voltage waveform. The waveforms

can be seen as voltages fed to comparator. If the reference voltage is higher than the carrier voltage, the upper valve is turned off. The duty cycle determines the output voltage as follows:

$$V_O = V_{DD} \cdot D, \tag{2.6}$$

where D is duty cycle and V_O is output voltage.

2.2.2 Full-Bridge

The full bridge or sometimes called H-bridge configuration consist of two legs sharing the same DC - rail. The midpoints of these legs are connected to the load and in the piezo application there are choke inductors attached to center point of both legs. The inductors can also share same with doubled area while winding copper material can be spared as less turns are needed. As in half bridge configuration, the upper and lower switch cannot be driven at the same time.

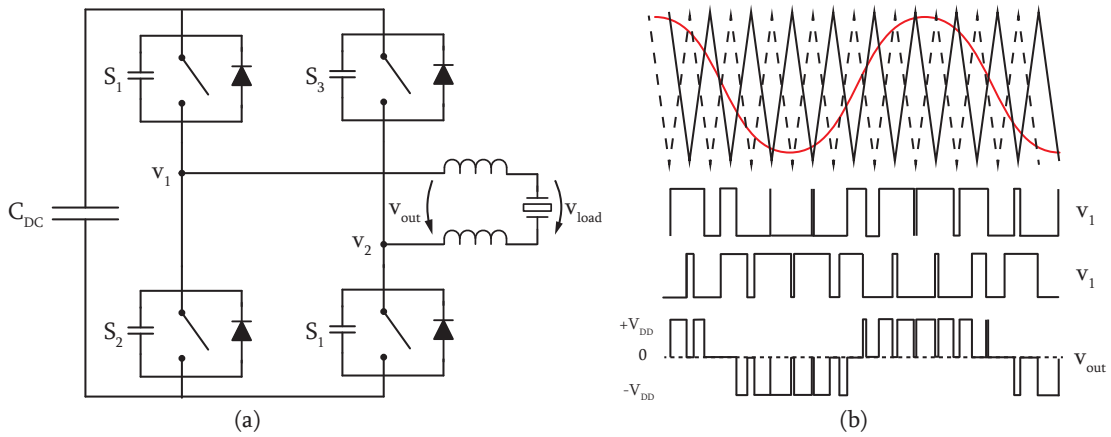

Figure 2.4: Full Bridge topology (a) schematic of the topology (b) PWM derivation for both legs and output

The output voltage of the full-bridge can be negative or positive DC-rail voltage or zero according to position of the valves.This is presented in Table 2.1. A positive DC-bus voltage can be applied to the load by switching the upper switch of the first leg and the lower switch of the second leg. In the same way a negative output voltage can be achieved by switching the lower valve of the first leg and the higher valve of the second leg. The other possibilities are activating both higher or lower

switches. This way the DC -bus voltage is not connected to the load, however, the current path is provided so that continuous mode can be achieved.

Table 2.1: Full bridge switching possibilities.

S_1	S_2	S_3	S_4	Output Voltage
1	0	1	0	0
1	0	0	1	+Vdd
0	1	1	0	- Vdd
0	1	0	1	0
0	0	0	0	0

The are two basic methods to provide switching patterns for the full bridge topology when PWM-modulation is utilized. In **bipolar method** the second leg is driven as complement to the first one. When the reference is above the carrier waveform, a positive rail voltage $+Vdd$ is applied to the load and while the reference is below the carrier, a negative rail voltage is applied to the load. The output voltage is similar to the half bridge topology and the voltage difference is high, which increases to the current ripple of inductive load.

The second modulation technology is so called **unipolar method** where different switching timings are provided for the legs. In the other words the legs are not switched at the same time but the control signals are generated independently. As the output voltage is voltage of the second leg subtracted from voltage of the first leg, the output varies between zero and Vdd, which is half compared to bipolar method. Secondly, the effective output switching frequency is doubled as the legs are controlled in 180° phase shift. Combining these features, the output filter can be designed to be much smaller and still provide wanted current ripple properties.

The switching waveforms can be achieved with several ways. Usually triangle carrier waveform is used but also sawtooth is possible. With modern micro controllers the sawtooth provide better PWM resolution. If triangle carrier waveform is utilized, the PWM can be generated by comparing a single carrier voltage with reference voltage and inverted reference voltages. The other way to achieve same result is to compare two carriers with 180 ° phase shift with the reference.

2.2.3 Multi-Level Topologies

As the output voltage rises, the blocking voltage of the semiconductor valves becomes the limiting parameter. Power semiconductors can be connected to series, how ever, there is few problems involved;

- uneven spread of turn on times
- uneven spread of leakage currents
- uneven spread of turn on delays

Even if the MOSFETs and IGBTs are said to be easiest to connect in series, some extra components are needed. [18, p.132-137] Compared to series connection and driving the valves with the same waveforms, the extra switching device can be controlled independently more output voltage levels can be generated. By dividing the output voltage transitions to smaller portions, the current ripple decreases and the load (piezo) voltage becomes smoother. On the other hand, switching component count usually doubles which increases manufacturing costs.

There are variety of multilevel DC-AC converter topologies available and the three most used ones are presented next.

In **Neutral Point Clamped** (NPC) topology has been utilized in medium voltage high power applications. It consist of four valves per phase leg sharing the DC-bus voltage. As in half bridge topology, the bus capacitor is spitted in half providing neutral point (0). Basic principle of NPC topology is shown in Figure 2.5. Center point of two highest and the two lowest switches are clamped to the center point of the DC-bus with a diode. While current can be drawn unevenly from the series connected bus capacitors through neutral point, neutral point voltage deviation may occur.

With a single phase leg there are three voltage possibilities; -$\frac{1}{2}V_{DD}$, 0 and $\frac{1}{2}V_{DD}$. The positive voltage is applied when the both upper valves are on and negative voltage is obtained while the both lower switches are on. A neutral zero voltage is connected through clamping diodes and the switches S_2 and S_3 depending on the current polarity. Voltage stress of a single switch is kept in $\frac{1}{2}V_{DD}$ when a proper switching pattern is used: the output voltage should not be switched between negative and positive polarity but through zero voltage commutation state. Similar to full bridge topology to output voltage is stated as $V_{out} = V_1 - V_2$ there is total of five voltage stages available.

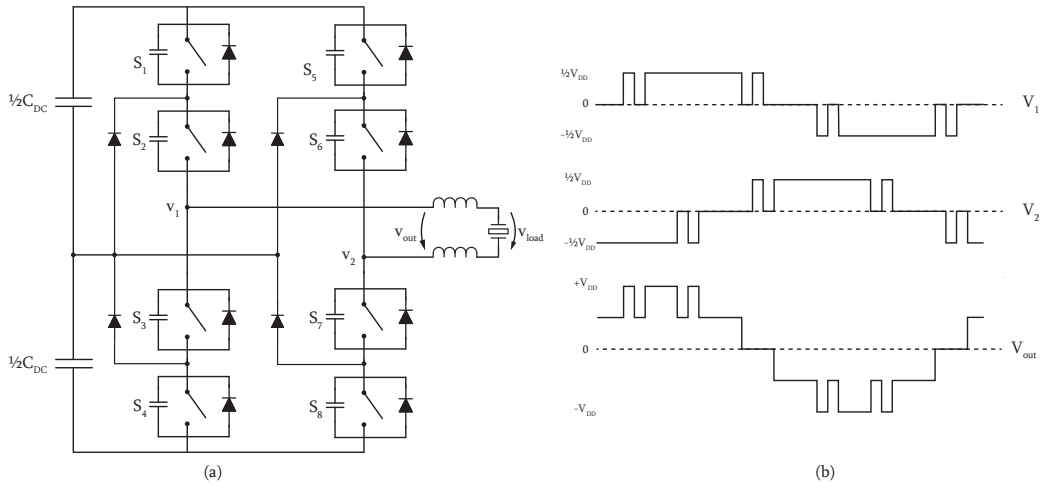

Figure 2.5: Neutral Point Clamped topology (a) schematic of the topology (b) switching pattern.

Cascaded H-bridge topology consists of multiple identical full-bridge (H-bridge) power cells. The main principle of the topology is presented in Figure 2.6. Outputs of the cells are connected in cascade to provide higher AC voltage and low THD. Power cells can be manufactured as one modular structure to decrease manufacturing cost. Every cell added to the system increases the voltage levels by two. For example seven level one phase inverter can be achieved with three cells. The Cascaded H-bridge (CHB) is a popular topology in high power medium voltage (MV) applications. [30, p.119-142]

Every switching valve has to withstand only voltage of input DC-rail. Output voltage rating increases when more cells are added to the system. Relatively high output voltage of over 3 kV can be achieved with normal 600 V rated valves by combining 12 power cells.

CHB topology requires relatively high component count. All the cells consist of four power switches needing own gate driver circuit. Also, every power cell must be equipped with own galvanically isolated DC power supply. Usually a phase shifting transformer connected to diode rectifiers provides multiple power sources while keeping the line-current harmonics at low level. [30, p.119-142]

There are two basic methods to generate the switching waveforms for the CHB converter; *Level-Shifted Multi-Carrier Modulation* (LSMC) and *Phase-Shifted Multi-Carrier Modulation* (PSMC). In the first method, the carrier waveforms are level shifted so that they are above each other. The amplitude of the reference signal is relatively higher than amplitude of a single carrier. All the carrier waveforms

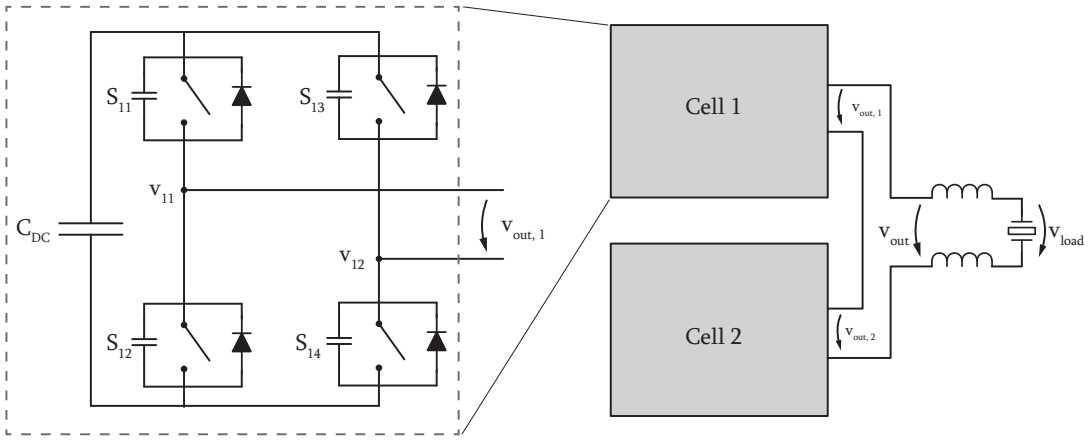

Figure 2.6: Cascaded H-bridge topology.

fit inside the amplitude of the reference signal. The LSMC method does not provide doubling of effective output switching frequency and the generation with microcontroller is more complicated.

PSMC method, illustrated in Figure 2.7, is similar to full-bridge unipolar control method, where both converter legs have their own carrier waveform. Carrier waveforms are phase-shifted 180 °. When multiple power cells are involved, carrier waveforms of an individual cells are similar phase-shifted by 180°. Carriers of different power cells can be calculated as:

$$\alpha_c = 180^\circ/m, \tag{2.7}$$

where the α_c is the phase shift of a single power cell and m is the number of power cells. When there is two power cells involved, the carrier waveforms between the cells are phase shifted by 90 °. It is noticeable that as with full bridge converter the effective output switching frequency was doubled, with multiple cascaded power cells the output frequency is derivated as:

$$f_{sw,out} = f_{sw,valve} \cdot 2m, \tag{2.8}$$

where the $f_{sw,out}$ is the effective output switching frequency, $f_{sw,valve}$ is switching frequency of a single valve and m is the number of power cells.

The voltage levels in CHB converter can be increased with uneven DC bus voltage distribution between the power cells. V_{DD} of the second power cell is doubled to $2V_{DD}$ and the maximum output voltage is $3V_{DD}$. The minimum voltage step is then V_{DD} and number of levels is seven when two power cells are utilized. Voltage

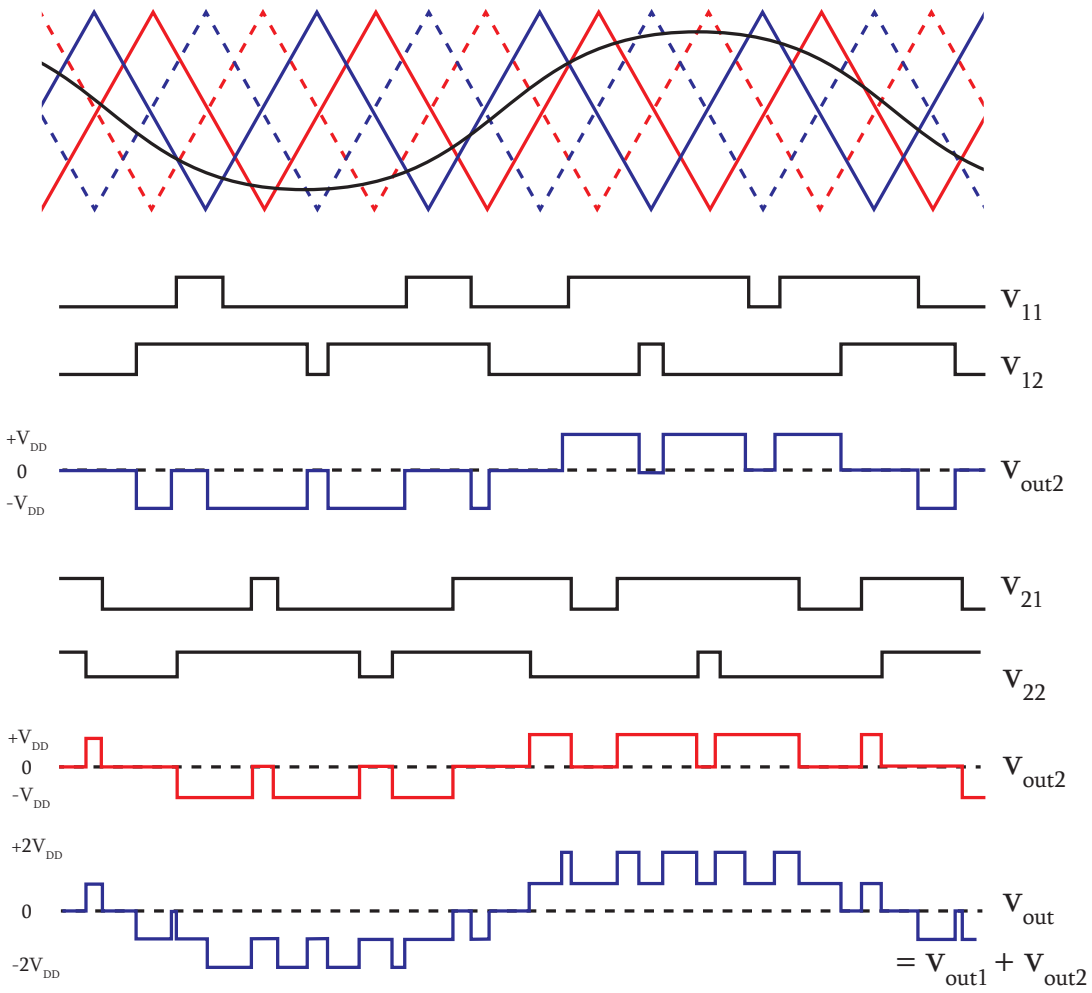

Figure 2.7: Cascaded H-bridge waveforms generated with phase shifted carriers.

levels of two cell converter can increased to nine by spreading the DC bus voltages with ratio 1:3. However, controlling such converter becomes even more complicated and the modular design aspect is lost. Therefore, the usage of uneven DC bus voltage is limited in industry applications. [30, p.119-142]

Flying Capacitor Converter (FCC) is not as frequently used topology as the previous ones even though it has some advantages. The converter is somehow similar to the Neutral Point Clamped converter. Instead of clamping diodes, FCC utilizes extra capacitor between the center points of two top valves and two bottom valves. A five level one phase topology is illustrated in Figure 2.8 (a). The basic

principle of the converter is that a single leg of the converter can provide an extra voltage level while the current path is going through the flying capacitor. Similar to NPC converter by adding two of these legs a five level DC-AC converter can be formed. [19]

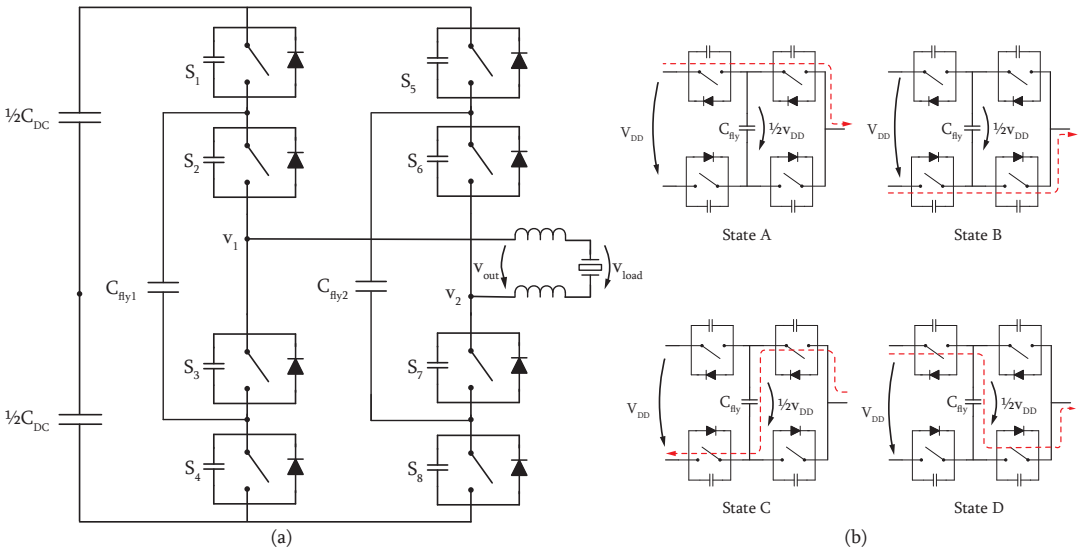

Figure 2.8: Flying capacitor converter topology. (a) Two leg one phase converter, (b) different stages of a single leg.

The Figure 2.8 (b) shows the switching states of a single leg. If referred to negative rail voltage the stages A and B are providing full rail voltage and zero voltage, respectively. Stages C and D provide half bus voltage according to current flowing direction. While stages C and D are used, the flying capacitor is charged and discharged. To keep the voltage of the flying capacitor inside some boundaries these two stages must be utilized evenly.

The FCC topology has it advantages while it doesn't need multiple isolated power supplies or camping diodes as the other converters. However the load current must flow through the flying capacitor, which produce some losses. Thus the type of the flying capacitor must be carefully chosen to minimize the losses. [19]

2.3 Components

In this chapter the basic component of power electronics are examined. The most crucial part of the power electronic application are the semiconductor valves, which

provide high blocking voltage and current carrying properties. On the other words these valves have high breakdown voltage and low resistance while conducting. These power devices are driven with gate driver circuit, which usually needs to be galvanically isolated. Also passive components such as DC-bus capacitors and output choke inductors are studied as they affect the performance of the driver.

2.3.1 IGBT

IGBT(Insulated Gate Bipolar Transistor) is a relatively new component. Fist commercial IGBT was published on year 1986 and currently it is the most important device in converter applications from hundreds of watts to few MW. IGBT combines advantages of both MOSFET- and BJT-transistors and the structure of device is very similar to the MOSFETs. The major difference is the added p-type layer on the collector terminal side. The device has similar high impedance gate as MOSFET does meaning it is easy to drive. The positive gate-emitter voltage V_{ge} introduces N-channel to the P-region such like in MOSFET. The voltage controls the base current of the PNP transistor. At the same time the added p-type region forms holes, which make the on-state voltage drop relatively low. The parasitic NPN-transistor along with PNP-transistor could form a thyristor if the base voltage of the PNP is drift away from emitter. This is prevented by reducing impedance of the P region and disperse majority of collector emitter current I_{ce} through the MOSFET. [18, p.99-100] [4, p.20-23]

There are two major categories of IGBTs; Punch Through (PT) and Non-Punch Through (NPT). PT-IGBT includes extra buffer N-type layer between drift- and p- layers that prevents failure against punch-through actions while the depletion region spreads all the way to the buffer layer. It also reduces the tail current when device is turning off by partially recombining the holes injected from p-region. PT-device is manufactured epitaxially etching just like MOSFET which is a expensive and slow method. Due the the buffer layer, the PT-IGBT has have reduced reverse breakdown voltage, which make them more suitable for circuit where diode applied.[18, p.101] [27]

NPT-IGBT does not have a buffer layer as discussed earlier and it has equal reverse and forward voltage blocking capabilities making it more suitable for AC applications. Also the manufacturing method is different than PT-IGBTs and there is no need to regulate the thickness of the drift-layer. NPT-IGBT have a negative temperature coefficient such MOSFET do. Almost all IGBTs rated over 600V are NPT-IGBTs. [18, p.101] [27]

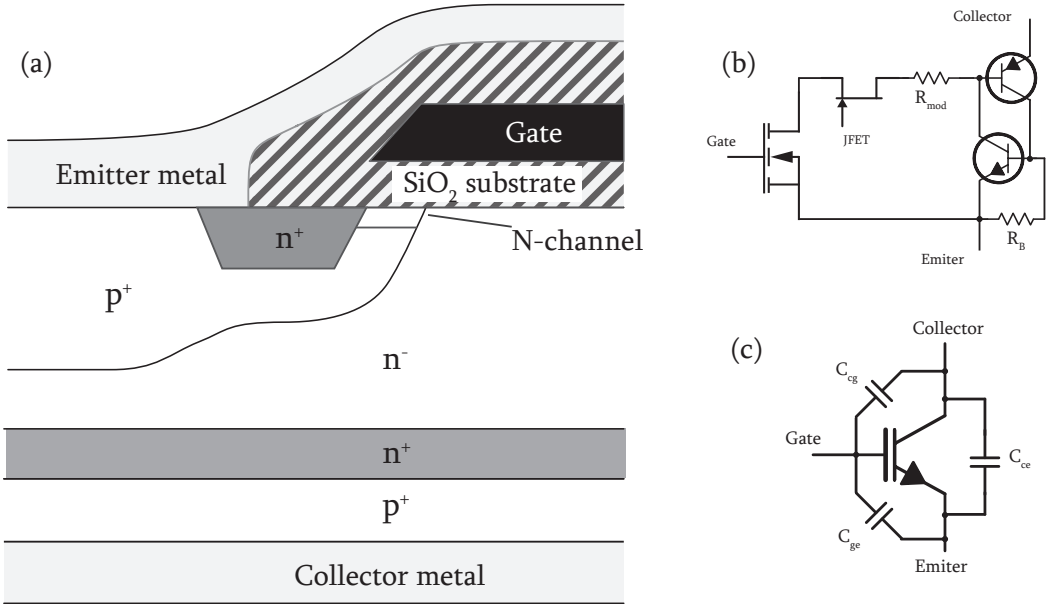

Figure 2.9: N-channel IGBT: (a) shows the construction of DMOS PT-IGBT, (b) is a corresponding schematic, (c) presenting the schematic symbols with the parasitic capacitances.

Manufacturers offer different types of IGBTs for different applications. By adding recombination centers, the tail current can be reduced, which makes the device more suitable for high frequency applications. On down side this increases the on state voltage drop that is undesirable property. Along with traditional DMOS structure, the trench technology has become available. TIGBT (Trench-IGBT) has lower on-state voltage drop and narrower cell pitch compared to traditional design. As disadvantage the TIGBT has lower blocking voltage than traditional one due the concentration of the electric field to bottom corner of the trench gate. [18, p.103] [15]

2.3.2 MOSFET

MOSFET (Metal Oxide Silicon Field Effect Transistor) are majority carrier devices meaning it is based on capacitive phenomenon. The current is not flowing through PN-junction like in BJT (Bipolar Junction Transistor) rather through a channel formed between drain and source terminals Figure 2.10 (b). The channel can be p- or n-type, however n-channel are more popular because of a lower on-state resistance. The theory behind FET (Fied Effect Transistor) has been available

some 20 year before the BJT was invented. Compared to BJT, MOSFETs are voltage driven, meaning they don't need constant energy to stay on. Instead the input capacitance needs to be charged, which draws high peak currents. Lack of minority carriers makes MOSFETs attractive in high frequency applications, where the switching losses dominate conduction losses. [26] [18] [10]

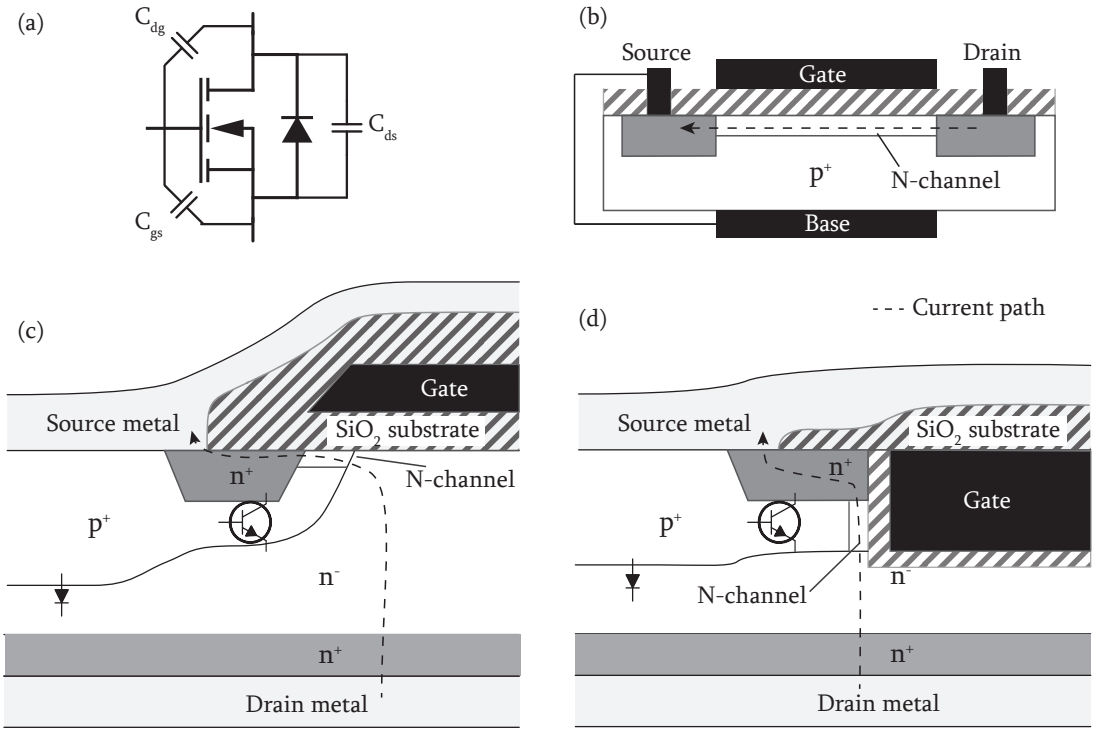

Figure 2.10: N-channel MOSFET: (a) shows the schematic mark with parasitic capacitances, (b) is construction of traditional MOSFET with drain and source on same side of wafer, (c) DMOS structure used in power MOSFETS and (d) is UMOS structure illustrating trench-gate insertion.

Power MOSFETs differ from normal MOSFETs by structure and are utilized in various applications such as automotive, switch mode power supply and motor control. Previously MOSFETs gate and source have been on same side of the wafer and the channel is formed between them. In power MOSFET the source and drain are on the different sides of the wafer meaning more cells can be constructed on same are. This decreases the on-state resistance $R_{ds(on)}$, which lower the conduction state losses. Figure 2.10 (a,b) presents the differences between the conventional and power MOSFET. Many new MOSFET devices utilizes trench technology in which the gate is inserted into a groove on silicon wafer. Figure 2.10 (d) shows

the trench structure where the current path is almost straight. Advantages using trench are lower $R_{ds(on)}$ due absence of parasitic JFET and smaller size, meaning more cells can be fitted on same area. On year 1998 so called CoolMOS FETs came to market. Relatively new technology improves blocking capabilities of MOSFET considerably without increasing the on-state resistance. All of these improvements have made power MOSFETS suitable for many power converter applications. [26] [18] [10]

Due the structure of the power MOSFET there are many parasitic components involved. Anti-parallel body diode is composed on PN-junction meaning the device cannot block current from flowing from source to drain. The diode shown in Figure 2.10(b,c) can be utilized in bridge configurations. However the body diode is usually quite slow and can be by-passed with a Schottky diode, with lower on-state voltage, placed between source and drain. Figure 2.10(b) also presents the parasitic BJT -transistor formed between source and drain. This transistor can become a problem on high drain-source voltage du/dt rates, that can turn the BJT on and eventually destroy the device. This phenomena is called "second breakdown" and can be prevented by decreasing switching speeds or by increasing doping density of the p body region. [18]

The parasitic capacitances are shown in figure 2.10 (a). Device data sheet usually announces following capacitances:

$$\begin{aligned} C_{iss} &= C_{dg} + C_{gs} \\ C_{oss} &= C_{dg} + C_{ds} \\ C_{rss} &= C_{dg}, \end{aligned} \tag{2.9}$$

where C_{iss}, C_{oss} and C_{rss} are input capacitance, output capacitance and trans conductance capacitance respectively. These capacitances are strongly negatively depended on drain-source voltage V_{ds}. Input capacitance is part of the gate driver circuit and has to be charged in order to turn the MOSFET on while the output capacitance determines what the rest of the circuit sees. C_{oss} forms usually some sort of resonator circuit along with stray inductance or load inductance which can cause unwanted voltage transient and overshoot on V_{ds}. This oscillator can be damped with external snubber circuit, if they become a problem. The trans conductance capacitance is highly involved in turn-on and turn-off events while some current is drawn through it causing so called Miller effect. Also the dependence on V_{ds} lower the charging and discharging rates of C_{iss}. [18]

MOSFETs have a negative temperature coefficient meaning that the on-state resistance $R_{ds(on)}$ increases while the temperature rises. Higher resistance reduces the current flowing in MOSFET cell causing it to cool down. Negative temperature

coefficient makes parallel connection of MOSFET quite easy and larger modules are assembled from multiple dies connected in parallel. However, the negative temperature coefficient can also be problematic if the cooling is not strong enough, causing MOSFET to heat up even more. If heat sink cannot transfer all the heat from the switching device, will it eventually overheat and be destroyed.[18]

Negative temperature coefficient also causes an other threat for the MOSFET called Electro-Thermal Instability that might force the device into linear region. The phenomenon is relate to local increase of the junction temperature which decreases $V_{gs(th)}$. This causes a rice of local current density which leads to increment of local temperature. In the end the current of whole MOSFET may be concentrated into current filament forming so called "hot spot". The hot spot causes the corresponding cells to loose control of the gate which leads to activation of parasitic BJT. The whole chain reaction will cause destruction of the MOSFET.

2.3.3 Wide Band Gap Devices (SiC MOSFET)

As requirements for power device evolve the silicon (Si) material approach its theoretical limits. Research has been made on new wide band gap (WBC) materials such as gallium nitride (GaN), silicon carbide (SiC) and diamond. WBG means that there is relatively large forbidden band between the conductive band and valence band.These materials have some superior electrical properties compared to silicon and they have been utilized in such applications which are not suitable for Si. WBG material parameters are compared in Table 2.2. Table reveals how the band gap of the WBG material is almost three times wider than silicons. Also the electric breakdown field and thermal conductivity are much higher. These parameters lead to many retentive characteristics that are discussed later on. [20]

Table 2.2: Wide band gap materials compared to silicon [20]

Property	Si	6H-SiC	4H-SiC	GaN	Diamond
Band gap, E_g	1.12	3.03	3.26	3.45	5.45
Electric breakdown field, E_c	300	2500	2500	2000	10000
Dielectric constant, ϵ_r^a	11.9	9.66	10.1	9	5.5
Thermal conductivity, λ	1.5	4.9	4.9	1.3	22

Silicon Carbide (SiC) MOSFET represents relatively new technology even though SiC diodes has been on market for over more than a decade. Wafer manufacturer Cree brought first generation SiC Schottky diode to the market on 2002 after discovering the material 1989. The voltage rating was 600V which was doubled

comparing to previous Schottky diodes.[20] In year 2011 Cree introduced the first commercial SiC MOSFET to the market. The voltage rating of the device was 1200 V. Other manufacturers such as SemiSouth, Infenion, GenceSiC and Fairchild soon followed with their SiC JFET and SiC BJT devices [11]. Due to new generations the price of the devices has reduced dramatically during the past few years. For example Cree has deliver the second generation devices which had improved the most of the design parameters such as $R_{DS(On)}$ and C_{oss}. In November 2012 Cree announced first commercial all-SiC half-bridge module including five 1200 V, 80 mΩ MOSFETs and five 1200 V, 10A Schottky diodes constructed on AlSiC baseplate. The module is rated on 100 A at 100 °C. Literature also shows race towards 1 MW class module been going on [25]. [9][16]

SiC switching devices have many advantages compared to conventional silicon based switching counter parts. The dielectric breakdown voltage (V_{BD}) of the carbide is almost 10 times higher that with silicon. For example if 1200V device is made of silicon, the drift layer has to be at least 100 µm of thickness to receive the desired blocking voltage. With SiC the thickness of the drift layer can be reduced to 10 µm while maintaining the same breaking voltage [8]. Thinner drift layer decreases the on state conducting resistance, which is one of the key parameters. [16]

Other advantage of SiC is better thermal conductivity meaning the junction to to case thermal resistance R_{jc} is reduced and the heat produced by the device is transferred out more efficient. Also, the junction temperature T_j of SiC can be higher compared to Si, which leads to better heat dispassion, because heat transfer is related to temperature difference given as:

$$H = \lambda A \frac{T_{hot} - T_{cold}}{L}, \tag{2.10}$$

where H is conducted heat, λ is thermal conductivity, A is conductive area, L is length of conductive area and $(T_{hot} - T_{cold})$ is the temperature difference [34, p.664]. Normally junction temperature T_j of the silicon device must be kept under 150 °C while SiC can operate temperatures up to 200 °C. [20] [25]

One of the major advantage of the SiC MOSFET compared to IGBT is the absence of the tail current, which increases the turn of losses. Tail current also increases the dead time needed between upper and lower device in half-bridge configuration. However the tail current provides some parasitic damping during turn-off state. Due to minor damping of the SiC, additional ringing and overshoot occurs which can even destroy the switching device. However SiC MOSFET has better avalanche ruggedness meaning is withstands short over voltages without breaking [8]. Special consideration has to be made while designing the current path and snubber circuit

especially if IGBT is directly replaced with SiC MOSFET. [5] [**?**]

Due to the better turn-on and turn-off performance of the SiC device, the switching frequency can be increased. This leads to smaller passive components such as output filter chokes and capacitors. This makes the converter more compact and power / weight ratio increases. On the other hand fast switching speed can also cause EMC problems due high di/dt and di/dt rates. [20]

SiC devices have also some disadvantages. Manufacturing cost of the SiC wafer can be up to 50 times more expensive than silicon wafer. On the other hand the production quality has been improved and currently even 150 mm SiC wafer can be produced.[11]

As shown in Table 2.2 diamond theoretical has the best characteristics of all WBG material. Nevertheless, processing temperatures of the diamond semiconductor are even higher than with SiC thus diamond is very hard material. Any commercial diamond solid-state switches has not been able to produce. However, there is some progress made and literature shows that diamond JFET and diode devices have been produced and tested in various temperatures in vacuum.[13]. [20]

2.3.4 IGBT/MOSFET Drivers

The purpose of the gate-driver is to set switching device from high-impedance state to low-impedance state and backwards. In order to do that driver has to charge parasitic capacitors in order to bring the gate voltage V_{gs} above the threshold voltage $V_{gs(th)}$. Driver also has to discharge capacitors in oder to turn off the device. Combining C_{gs} and C_{rss} or 'Miller' capacitances we get C_{iss} which is the total input capacitance that is also called C_{gate}. IGBTs input state is almost identical to MOSFETs, driving of both devices is very similar. Parasitic components are reported similarly only terminals have different names as shown in Table 2.3. [2]

Usually the driver is able to reach gate voltage close its supply voltage V_{dd}, which is chosen high enough to deliver MOSFET/IGBT to saturation. The switching device is considered to be fully open while its in saturation state. In off-stage V_{gs} has to be under $V_{gs(th)}$. If bipolar gate supply voltage is used, the gate voltage is driven on negative polarity. Driving gate to negative bias is used especially in noisy environments to ensure off-state while external disturbance occurs. Also high du/dt transients can cause current to flow through C_{rss} and C_{gs} which can produce voltage spikes to the gate voltage. These unwanted spikes can rise above the $V_{gs(th)}$ and cause the device to turn on unintentional. By minimizing the reverse

Table 2.3: Similar parameters of IGBT and MOSFET

IGBT parameter name	IGBT symbol	MOSFET paremeter name	MOSFET symbol
Collector emitter voltage	V_{ce}	Drain source voltage	V_{ds}
Collector current	I_c	Source current	I_s
Gate emitter voltage	V_{GE}	Gate source voltage	V_{gs}
Gate-to-emitter charge	Q_{ge}	Gate-to-source charge	Q_{gs}
Gate-to-collector charge	Q_{gc}	Gate-to-drain charge	Q_{gd}

transfer capacitance C_{rss} the phenomenon can vanish. Use of negative gate voltage increases the margin between turn-off gate voltage and threshold voltage, which can prevent shot-through from happening. IGBT is usually driven between +15 V and -15 V to reduce switching losses. SiC MOSFET should be driven from - 5 ..- 2V to +20V. With SiC MOSFET the negative gate drive is highly recommended because of relatively low $V_{gs(th)}$ of 2.5 V. [31] [2] [27]

Modern switching devices set high demands for the gate-drive circuit. Relatively wide voltage swing, high gate charges, fast switching speeds and increasing switching frequencies impose challenges to the driver. Peak current during switch on and off could rise up to 30 A. The peak current can be calculated from basic capacitor current equation as follows:

$$i_C = C\frac{du}{dt} \Rightarrow i_{drv,p} = C_{gate}\frac{V_{dd}}{T_{turn}}, \tag{2.11}$$

where $i_{drv,p}$ is the peak current of the driver V_{dd} is the supply voltage and T_{turn} is the turn on/off time. The current driver needs is drawn from the by-pass capacitor of the driver that should also be carefully chosen and placed as close to driver as possible. Additionally these capacitors should have low equivalent series resistance and inductance to be able to provide such peak currents. The internal output resistance of the driver should be kept as low as possible to prevent driver from overheating. Also power needed for driving switching device could rise to multiple watts. The gate charge losses are given as:

$$P_{gate} = V_{CC} \cdot Q_g \cdot f_{sw}, \tag{2.12}$$

where V_{CC} is drivers supply voltage, Q_g is total gate charge of the switching device and f_{sw} is the switching frequency. It is also noticeable that Q_g f_{sw} corresponds to

average gate current. The power consumed by the driver using MOS output state can be calculated as follow:

$$\begin{aligned} P_{Drv(On)} &= \frac{1}{2}\frac{R_{Hi} \cdot V_{Drv} \cdot Q_g \cdot f_{sw}}{R_{Hi} + R_{Gate} + R_{Gate,Int}} \\ P_{Drv(Off)} &= \frac{1}{2}\frac{R_{Low} \cdot V_{Drv} \cdot Q_g \cdot f_{sw}}{R_{Low} + R_{Gate} + R_{Gate,Int}} \\ P_{Drv} &= P_{Drv(On)} + P_{Drv(Off)}, \end{aligned} \tag{2.13}$$

where R_{Hi}, R_{Low}, $R_{gate}$and $R_{gate,int}$ are the high-side (source) and the low-side (sink) resistances of driver, the external gate resistance and the the internal resistance of switching device respectively. The total power produced in the driver should not exceed the power dispassion of the driver. Figure 2.11 presents impedances in driver circuit. [21] [2]

The external gate resistor circuit should be chosen carefully. Gate circuit always includes some stray inductance caused by conductors or tracks on PCB. The external resistor should be large enough to damp resonator circuit, formed between stray inductance and input capacitance of switching device, from unwanted ringing effect. On the other hand the R_{gate} regulates the gate current and slows down rise and fall times of the switching device. To achieve high switching speeds the stray inductance should be minimized by placing driver as close to the device as possible. It is stated that distance increases the inductance in rate of 5 - 10 $\mathrm{nH\,cm^{-1}}$ [18, p.214]. Also the gate traces should be evenly placed on PCB and as close to each other as possible. Methods for minimizing stray inductance is discussed in Section 2.4. Needed damping can be calculated as follow:

$$\begin{aligned} \varsigma &= \frac{R_{gate,tot}}{2}\sqrt{\frac{C_{gate}}{L_{stray}}} \geq 1 \\ \Rightarrow R_{gate,tot} &\geq 2 \cdot \sqrt{\frac{L_{stray}}{C_{gate}}}, \end{aligned} \tag{2.14}$$

where $C_{gate,tot}$ is total gate resistance, C_{gate} total device capacitance and ς damping factor of the gate drive circuit. Figure 2.11 shows parasitic and internal impedances in the driver circuit. [5].

Also some sort of protection such as under voltage protection should be taken into consideration. If the V_{dd} of the driver drops below the desired voltage, the switching device might end up to linear region and overheat. Other useful protection is short-circuit / over current protection. Usually this is done by monitoring the

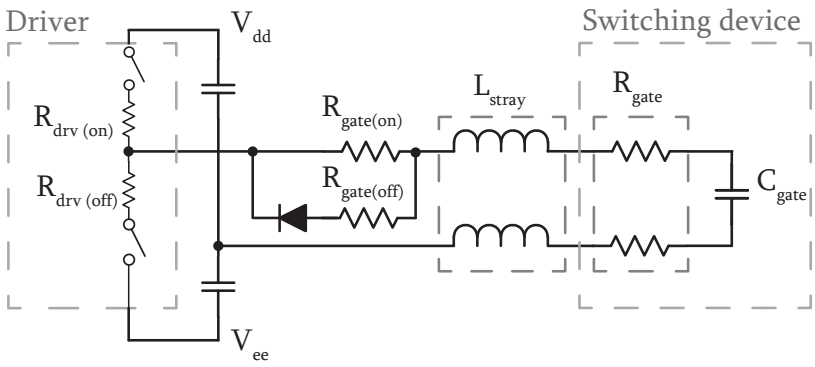

Figure 2.11: Gate driver circuit impedances.

voltage across the switching device (V_{ce} or V_{ds}). If short circuit occurs, the voltage across the the device increases rapidly during on-state. Sometimes protection is integrated in driver IC to minimize external components. [21]

Almost in all chopper converter application some sort of half-bridge or similar configuration is utilized in which gate potential varies. In these type of setups a galvanic isolation or a level-shifter is needed to bring gate signals to midpoint of half-bridge for example. Beside gate signal power must also be brought to the potential of the upper switch. Usually logic control ground is referred to the negative rail potential which makes low side switches relatively easy to drive. If no galvanic isolation is needed, quite simple bootstrap + level-shifter configuration could be used. However if galvanic isolation is required, opto-couplers along with isolated converters or isolating transformer would be the choice. In Figure 2.12 three different drivers topologies are presented. [21]

As stated before *bootstrap gate driver* doesn't provide galvanic isolation meaning that the gate signal is transferred to reference potential of high switching device by level-shifter. In Figure 2.12a the driver topology is presented. The supply voltage of higher switch is provided by so called bootstrap condenser C_{boot} and bootstrap diode D_{boot} with additional resistor R_{boot}. The D_{boot} has to have high blocking voltage. The C_{boot} is charged while the lower switch is turned on and the center point of the half-bridge is close to GND. Then the lower switch is turned off the D_{boot} turns to reverse biased and current through it is blocked. While the upper switch is turned on the energy in C_{boot} is used to charge the gate capacitor. While the charging of the C_{boot} is done during on-state of the lower switch it is not possible to achieve duty cycles close to 100 %. [2] [21]

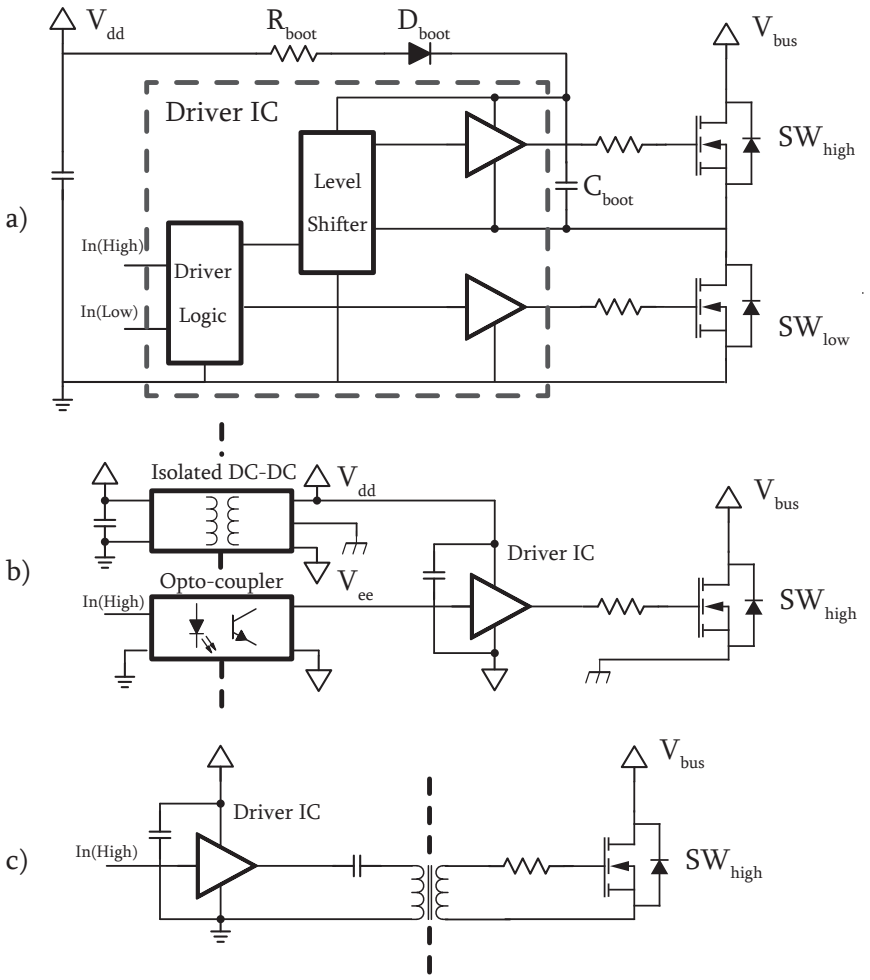

Figure 2.12: Different gate driver topologies: a) boot-strap topology with level-shifter circuit, b) isolated opto-coupler with isolated DC-DC converter, c) transformer based isolation driver.

An opto-coupler along with an isolated power supply provides galvanic isolation that is needed in many topologies such as matrix converters and bi-directional switches. In opto-coupler the input is usually a infrared LED that is emitting light to the photo detector through transparent insulating film [14]. Typically in switching mode converter opto-couplers with reinforced insulation are utilized[32]. Opto-isolators provide relavely easy interface with controller and can be used with frequencies in MHz range. As a drawback the opto-coupler adds additional propagation delay to the driver circuit. Additional capacitance between input and output can cause problems when the du/dt rates between input and output rises above 100 $\mathrm{V\,ms^{-1}}$. The output opto-coupler cannot drive the power valve by itself which makes additional gate-driver circuit compulsory. There is also opto-gate-driver circuits on market that combines the both devices into one integrated circuit. However, these devices provide only relatively low peak gate current (up to 2.5 A) and long propagation delays. Opto-coupler can also used to bring fault signals back from the driver. [1] Fiber optics are also widely used especially in modern frequency converters. Sometimes the optic fiber is the only choice if the isolation voltage is hundreds of kV. Isolated power supply utilizes transformer to form a galvanic isolation between the primary and secondary. Push-pull, Flyback, Forward or similar converter topology can be used. Negative supply voltage is fairly trivial to produce with such converters. There is also isolated voltage DC-DC converters available on market but one should be careful with the isolation voltage ratings, which are usually quite low. [21] [18]

Another way to provide galvanic isolation for the gate is to utilize *gate driver transformer(GDT)*, where the gate is charged through pulse transformer. This method is frequently used in switching power supplies and can be quite efficient if the transformer is designed carefully. The GDT provides high peak currents during turn-on and turn-off while minor average power is delivered through the transformer. Figure 2.12(c) shows a simple configuration for the transformer coupled gate driver, where the driver IC is attached to the transformer through resistor R_c and coupling capacitor C_c. Purpose of C_c is to provide alternative voltage across the transformer primary, that will reset the core. Voltage of C_c is determined as: $V_{C_c} = DV_{dr}$, where D equals to duty cycle and V_{dr} is the driver voltage. Without flux resetting the core material could saturate due permanent DC-voltage across the core primary. GDT could be also driven with double ended configuration in which the transformer can operate in both fist and third quadrant of H-B plane. [21] [2]

The main advantages while using GDT are practically zero propagation delay and absence of isolated DC/DC converter. The minimal propagation delay allows accurate switching especially when high switching frequencies are used. Isolated DC/DC converter rises the price of the device, which can be essential especially

with high volume applications. The transformer can also provide several outputs for multiple switching devices making it possible to drive simultaneous pulses to different switches.

2.4 DC-Rail

2.4.1 DC Capacitors

The capacitors provide energy storage for the switch mode converters. Energy of the capacitor can be calculated from equation:

$$E_c = \frac{1}{2}CV^2, \tag{2.15}$$

where E_c, C and V are capacitors energy, capacitance and capacitor voltage respectively. When the load capacitor is charged, voltage of the rail capacitor should not drop drastically. The rail voltage after load capacitor charging can be estimated if an assumption is made, that there is no energy lost in converter.

$$\begin{aligned} E_{rail(end)} &= E_{rail(begin)} - E_{load} \\ \Rightarrow V_{rail(end)} &= \sqrt{V^2_{rail(begin)} - \frac{C_{load}}{C_{rail}} V^2_{load(begin)}}, \end{aligned} \tag{2.16}$$

where the $E_{rail(begin)}$ is the nominal DC-rail voltage and $E_{rail(end)}$ is the DC-rail voltage after the load is charge while $E_{Load)}$ is the energy needed to charge the load. $V_{rail(end)}$ and $V_{rail(begin)}$ are DC-rail volatages before and after load chaging the load. C_{load} and C_{rail} are load capacitance and DC-rail capacitance respectively. When the load is charged, the current is dawn form the DC-rail which voltage will drop.

2.4.2 Bus and Layout

In power electronics the layout should not be overlooked because at high frequencies it can be considered as an independent component. A power converter includes switches that chop for example voltage with high du/dt rates. These fast occurrences consist of various current and voltage harmonics that affect the Electro-Magnetic Compatibility(EMC) and over all operation of the circuit. While the switching speeds have risen due the new generations of switching devices, also more and more

consideration is required towards parasitic elements of PCB layout or copper rails. [18, p.214-215] [26] [7]

There are few areas where the conductor placement is critical. One of them is connections between high voltage switch and the DC rail. In ideal world the capacitor bank and the switches are connected with a short-circuit while in real world the conductor has its own impedance. Especially the inductance in the conductor should be minimized while it forms a resonant circuit with power switches output capacitor. When AC-voltage is applied, resonator revives and causes voltage and current ringing and over-shoot. This high voltage ringing is usually shown in EMC tests and over-shoot of V_{ds} or V_{ce} can destroy the switching device. Inductance formed in between capacitor bank and the power switch is called stray inductance and it can be optimized. [7]

The most obvious way to reduce inductance is to place components as close to each other as possible. Usually this has been taken into consideration while designing the layout. Other method to cut the inductance is to cancel out the magnetic fields of the conductor produced. When current is applied to conductor it forms a magnetic field according to right hand rule. If another conductor, where the current is flowing to the opposite direction, is placed nearby, the magnetic field are also colliding. This causes the fields to cancel each other out, decreasing the inductance. The inductance per length of conductor bars stacked parallel is given as:

$$L/l = \mu_0 \frac{d}{w}, \tag{2.17}$$

where the μ_0 is the vacuum permeability, d is the distance between conductors and w is the width of the conductors. The distance between the conductors can be reduced within boundaries of breakdown voltage. For example the short term dielectric breakdown voltage of the FR4 is 20 $\mathrm{kV\,mm^{-1}}$.

2.5 Output Inductor

The purpose of the output current choke is to limit the current variation during the switching period. There are commercial chokes available in many forms. However, there is such a long list of parameters involved that usually a custom designed inductive component is needed.

A choke inductor usually consists of a core and copper winding. While current is flowing in windings, a magnetic field H is formed around the wire. The magnetic core usually has high permeability μ and magnetic flux density B is higher inside

the core compared to outside. The relation is formed as:

$$B = \mu H, \tag{2.18}$$

where the permeability can be split into permeability of vacuum μ_0 and relatively permeability μ_r as:

$$\mu = \mu_0 \mu_r, \tag{2.19}$$

where μ_0 is constant and μ_r is depended on the material. Air has μ_r close to one and iron has value of several thousands. Magnetic materials usually have linear region in B/H curve called linear region. However the μ_r of magnetic materials doesn't stay constant and decreases when high H field is applied causing saturation of the magnetic material. In saturation, flux density doesn't increase as much as in linear region. Core materials have some maximum flux density that should not be exceeded or otherwise the current flowing in wingding starts to rise rapidly.

Magnetic path has magnetic reluctance Λ, which is determined as:

$$\Lambda = \frac{l}{\mu A}, \tag{2.20}$$

where l is the length of the magnetic path and A is the cross section area of the path. As magnetic material usually have high permeability, an air gap is utilized to increase the reluctance of the magnetic circuit. Then the total reluctance is the sum of different components similar to series resistances of electrical circuit. Magnetic flux is determined as follows:

$$\phi = \frac{Ni}{\Lambda}, \tag{2.21}$$

where N is the number of turns around the core and i is the winding current. Ni is also called magneto motive force. A choke has its own self inductance which is defined as:

$$L = \frac{N\phi}{i} \tag{2.22}$$

When the ϕ is substituted with flux Equation (2.21) inductance is:

$$L = \frac{N^2}{\Lambda} \tag{2.23}$$

It is noticeable that inductance is not determined by current flowing through it. However, when current flows and flux density rises, permeability changes. In linear region the inductance of the choke is constant but on saturation region, the inductance collapses.[17, p.46-52]

There are many core materials available on market and in some solutions the core can be replaced with air. Inductance value, maximum current and switching frequency are the main parameters and core losses are acting an important part when choosing the material.

Ferrite materials are widely used in high frequency applications. Ferrites have high electric resistivity which make them resistant for eddy current losses. On the other hand, ferrites have relatively low saturation flux density of 300 mT and saturation knee is quite hard.

Iron Powder cores are made of small iron particles that are isolated from each other. Thus isolation, those materials have high electrical resistance and are suitable for high frequencies. With iron powder core an additional air gap is not usually needed because there is small gap between the iron particles. [17]

Chapter 3

Simulations

Simulations were made with LTspice software provided by Linear Technology. LTspice is free SPICE (Simulation Program with Integrated Circuit Emphasis) program that is suitable for testing and simulate electronic circuits. Originally SPICE software was developed for simulate integrated circuits at University of California, Berkley. Majority of component manufacturers provide SPICE -models of their components for free that makes it possible to test circuits with corresponding components. The software includes basic circuit components and it is relatively easy to combine new ones. There are several models which can be modified by adding the right values from the components data-sheet. [17, p.69]

Several simulations were made to gain better understanding of the topologies. The main considerations were current and voltage waveforms of the load. Also gate voltage is one of the main concerns due the high du/dt values of the V_{ds} which causes unwanted voltage transients on gate voltage.

3.1 Three-Level Full-bridge

The topology consist of one full bridge construction described in Section 2.2.2. In order to achieve total of three voltage levels a unipolar PWM switching method is utilized. Also the effective output switching frequency is doubled compared to switching frequency of a single valve. The output voltage can be as high as the DC-bus voltage which means that in order to achieve 1 kV the rail has to be charged above that one kilovolt. DC-rail voltage must be higher because of the dead time involved limiting the maximum and minimum of the duty cycle.

Table 3.1: Parameters of full bridge simulation.

Parameter	Value
DC bus voltage	1200 V
Dead Time	0.6 µs
Output Inductance	1200 µH
Switching frequency of single leg	100 kHz
Output switching frequency	200 kHz

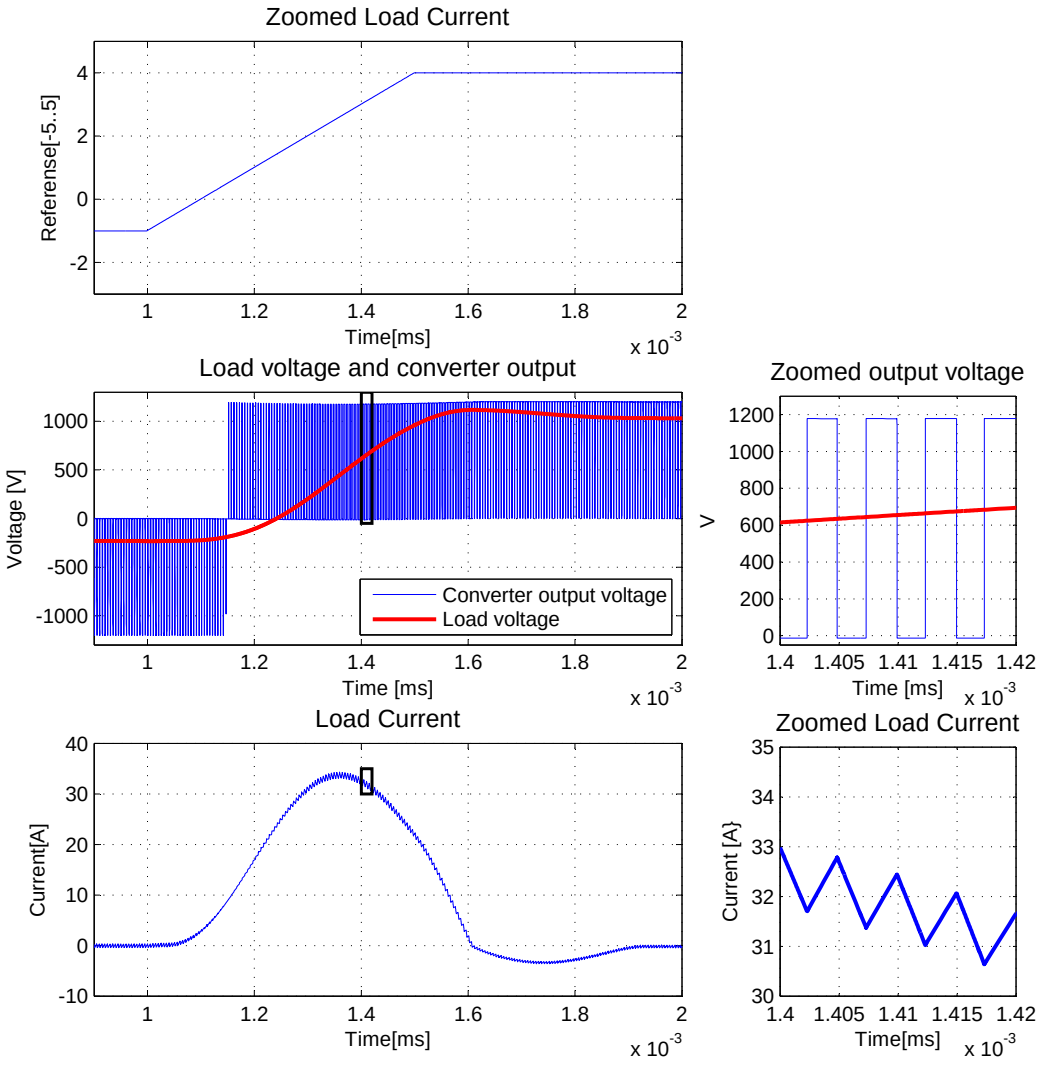

Figure 3.1: Open-loop performance simulations of the Full-bridge topology.

Simulation result is illustrated in Figure 3.1. As assumed, the effective output switching frequency is doubled compared to switching frequency of a single valve. The three voltage levels are shown and with the zoomed areas the relation between voltage and current can be viewed. Because of the open loop control, the output voltage overshoots close to 200 V over steady state. With feedback controller the overshoot should be kept within few percentages.

With such a high choke inductance value, the output current ripple is kept within 1 A. However, the current does rise relatively slowly because of the high inductance value. In order to control the current more precisely, the output inductance should be minimize.

3.2 Biased Three-Level Full-Bridge

TThe output voltage can be biased continuously, in order to utilize the full output swing of the full-bridge converter. An isolated power supply with a capacitor provides a path for the load current. This way the whole voltage swing of the full bridge converter can be utilized. While the whole load current flows through the bias supply capacitor, a low ESR value should be chosen in order to minimize the losses.

When output voltage is constantly biased, DC-bus voltage can be decreased compared to the full-bridge converter. A lower DC-bus voltage makes usage of 1200 V switching devices possible. Also, decreased voltage swing makes smaller inductance value possible.

Table 3.2: Parameters of biased full bridge simulation.

Parameter	Value
DC bus voltage	720 V
Bias voltage	380 V
Dead Time	0.5 µs
Output Inductance	800 µH
Switching frequency of single leg	100 kHz
Output switching frequency	200 kHz

Simulation results are gathered in Figure 3.2. The load voltage acts quite nicely even though only open loop control was utilized. The three voltage levels are shown

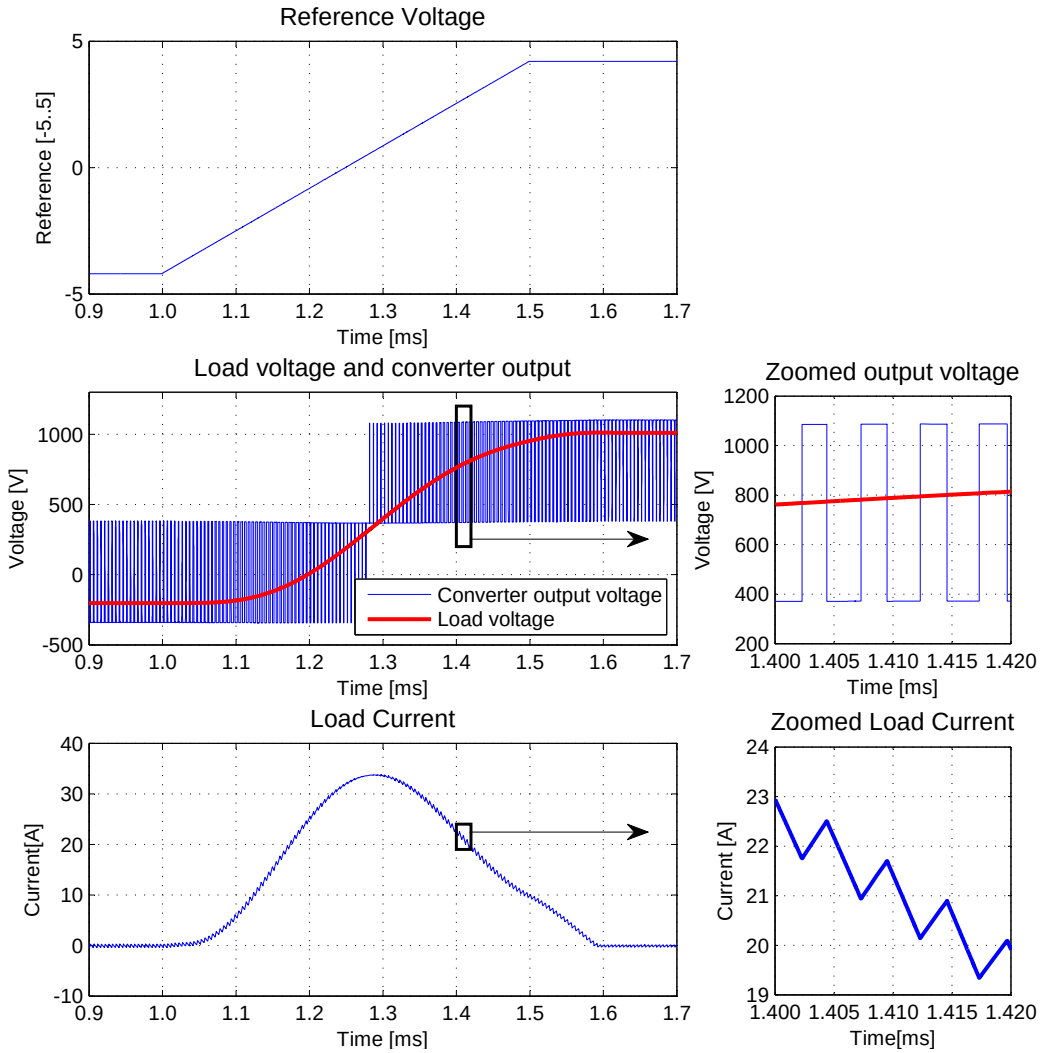

Figure 3.2: Biased full bridge simulations. Converter output is also biased as much as the bias voltage.

in the converter output voltage. The output voltage is biased to illustrate the affect of bias voltage. There is 0.1 ms delay between the reference and the load voltage.

The current waveform acts as expected. The ripple current stays withing 1 A.

3.3 Five-Level Cascaded H-Bridge

The construction includes two cascaded full bridge topologies in series. The PWM signals were constructed by comparing sawtooth carrier waveforms with the reference. Due the higher effective output frequency, the output filter could be smaller. Also the bandwidth of the converter increases, when the resonance frequency increases.

In Figure 3.3 a ramp waveform is fed as reference while the output voltage and piezo voltage are examined. Also load voltage is obtained in order to view the ripple current. The rise time was set to 0.5 ms. Simulation was made in open loop and no control was used. Because of the dead time involved, the DC rail voltage must be little higher than half of the output voltage needed.

Table 3.3: Parameters of cascaded H-bridge simulation.

Parameter	Value
DC bus voltage	600 V
Dead Time	0.5 µs
Output Inductance	600 µH
Switching frequency of single leg	100 kHz
Output switching frequency	400 kHz

From simulation it can be seen that four of five voltage levels were utilized while the output voltage rises from 250 V to 1 kV. In this application negative output voltage does not need to exceed 250 V. Voltage difference between the levels is the DC-bus voltage as assumed. There is 0.1 ms delay between the reference and the output voltage waveforms.

While the current waveform is examined, the amplitude rises rapidly to almost 37 A. The current ripple stays under 1 A.

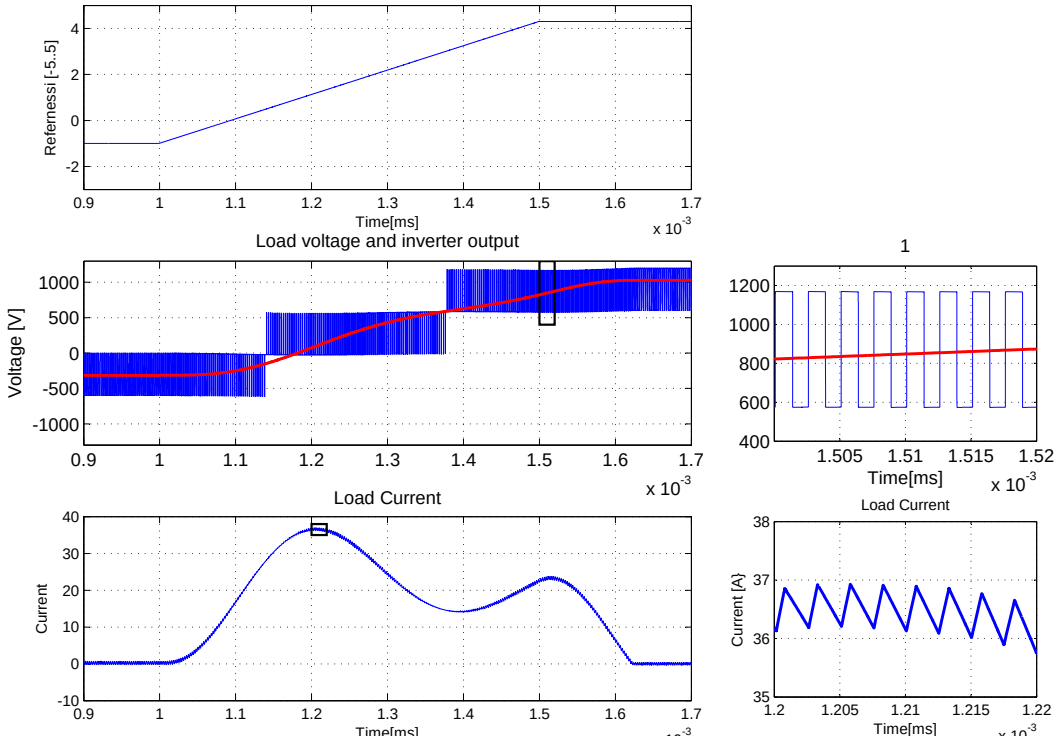

Figure 3.3: Simulations of open-loop performance of five-level H-bridge topology. On right hand side the the voltage and current waveforms are zoomed.

3.4 Simulation Summary

Usage of a simulator software is a good approach in order to understand the topology behavior. Simulations can also provide information which does not stand in the literature.

Three different concepts were simulated. All the topologies have advantages and disadvantages. A simple full bridge converter provide relatively good result. However usage of such a converter requires switching valves with higher blocking voltage than the rest of the topologies. Biased full bridge is an interesting concept. The full potential of the full bridge converter can exploited while DC bus voltage and output inductance can be kept relative low. On the other handling, an extra isolated DC bias voltage increases the complexity and the cost.

A five level cascaded H-bridge topology provides many advantages while it is the most complex topology. Component count is high because of multiple H-bridges and isolated power supplies. Only four voltage levels of five could be exploited

while the output voltage varies between - 200 and 1 kV.

The most promising result were obtained with biased full bridge and cascaded H-bridge converters.

Table 3.4: Parameters of cascaded H-bridge simulation.

Parameter	Full Bridge	Biased Full Bridge	Cascaded H-bridge
DC bus voltage	1200	720	600
Output inductance	1200	800	400
Complexity	Low	Medium	High

Chapter 4

Design

At the start of the prototype development phase, there was some specifications to be defined. The power supply should be able to drive high voltage piezo stack with relatively high current. The high voltage and high switching frequency set certain requirements for the system. The majority of the switching devices are too slow or the current and blocking voltage ratings are too low. The main idea was to use multilevel converter. With the same prototype board also biased full bridge converter could be tested. While using these topologies, the voltage stress of the switching device could be kept inside safety boundary. While utilizing phase shifted carrier waveforms and unipolar switching method, the effective output frequency can be multiplied.

The main concept is to have cascaded multilevel converter to provide bipolar voltage for the piezo actuator. Also the energy recovering from the piezo should be possible. The piezo voltage and current were measured to provide feedback for the controller. In Figure 4.1 the design is illustrated.

The original idea was to have majority of soldered to one printable circuit board (PCB) and two daughter board for micro controller and measurements. However, the design was changed after some of the components turned out to be under dimensioned. The discrete switching valves were changed to a half-bridge module along with the gate driver circuit. In Appendix **??** two pictures of the prototype are shown.

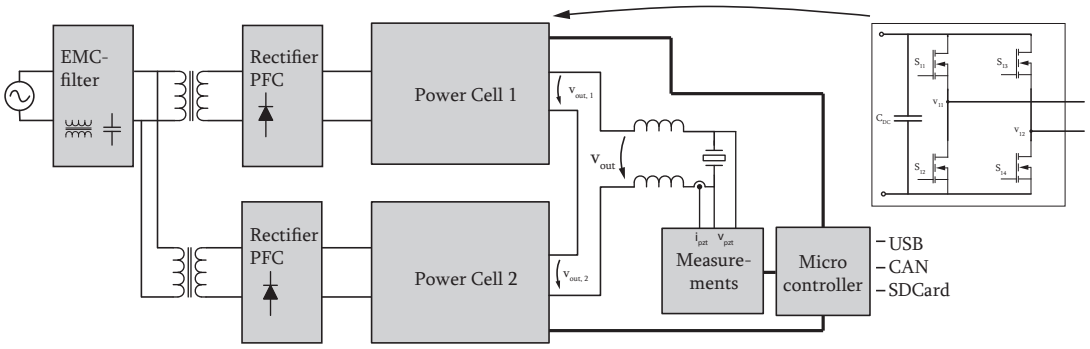

Figure 4.1: Prototype design.

4.1 H-Bridge

The full bridge section is based on SiC MOSFET half bridge modules **CAS100H12-AM1** provided by Cree. SiC MOSFET technology provide fast switching times needed in the application. Also the conduction and switching losses are kept minimum with multiple dies connected parallel inside the module. On the other hand the input capacitance C_g rises while parallel dies are increased. The high input impedance sets high demands for the gate driver circuit.

In this design a ready made gate driver board made by Cree was used. The driver circuit could provide peak current of 13 A and the output impedance is as low as 1 Ω. The driver boards were directly connected to the module gate signal pins with shortest leads possible to minimize the stray inductance. The gated driver boards utilize opto-coupler isolation between the input and output, which causes propagation delay, that should be taken into count.

The MOSFET modules were attached to the aluminum rod that transfers the heat from the module. A isolating thermal material was attached between the rod and the module. MOSFETS and diodes inside the module are already isolated from baseplate with dielectric. Heat sinks with option for peltier cooling elements were fastened to the aluminum rod.

The DC bus capacitors were placed as close to the MOSFET -modules as possible, to minimize stray inductance in the buss. Low ESR and ESL capacitors **E61** by Electronicon were used. Three capacitors forms a capacitor bank and low inductance copper rails connects modules and the capacitors leads together. The rails were stacked parallel in order to minimize the stray inductance by canceling out the magnetic fields.

4.2 Measurements

Voltage and current measurements were made with a separated daughter board. Both measurements were isolated because the load (piezo) is not coupled to any of the rail potentials.

The voltage measurement were done with an analog opto-isolator that includes two photo detectors, one for output and other for feedback. The current of input LED is controled with a PNP transistor which base terminal is fed by op-amp output. The feedback current from photo detector is connected to op-amp input through shunt resistor in order the have negative feedback. The voltage of the piezo actuator is divided with a differential resistor network top have voltage suitable for differential op-amp circuit.

After the analog opto-isolator, the output current is turned into voltage signal with resistor feedback of op-amp circuit. Because the measurement board is connected to main board with a cable, a differential output op-amp is used to have voltage information traveling without ground reference. Therefore the voltage information is not disturbed by the current flowing in the ground wire of the cable.

Current measurement is done with a open loop hall sensor manufactured by LEM. The measurement range of the sensor is -50 A to 50A. The sensor has voltage output which is fed to the different output amplifier providing two output in opposite phases.

From the measurement daughter board the differential signals were brought to the main board with twisted par cable. On the main board a differential amplifier combines differential signals to single ended a microcontrollers analog to digital converter samples the signal.

4.3 Microcontroller

Control of the power supply was implemented using 32-bit Texas Instruments TMS320F28035 microcontroller (MCU). The MCU combines of main processor (CPU) and co-processor called Control Law Accelerator (CLA). These processors share part of RAM -memory for communication purposes and in additional to that CLA has its own memory space . Main processor can control all the peripherals while CLA can control only ADC and PWM blocks.

In Power Supply application CLA could be dedicated for high speed control loops while the main processor is handling communication and other tasks. CLA is also capable to perform floating-point calculations making it ideal for performing control algorithms. CLA performs so called tasks which can be triggered by the Main processor, PWM or ADC blocks and the co-processor can perform independently form main processor.

In this work the controlling of the power supply was design quite simplistic. Reference curves for voltage and current were calculated with a MATLAB script and then inserted to Flash-memory as lookup-table. These table values are the fed to CLA processor through shared RAM and updated on every switching period. A block diagram of the controller is presented in Figure 4.2.

ADC-converter samples output voltage and current simultaneously and after five samples calculates an average value. These values along with reference values are fed to the CLAs control loop, where error terms and offsets are calculated. Lastly the result is limited and set as upcoming PWM-counter value.

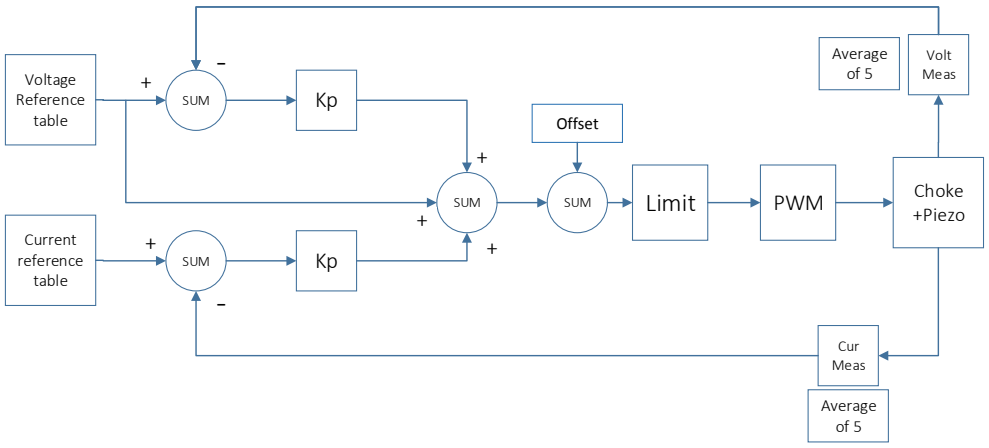

Figure 4.2: Block diagram of controller.

For debugging and external controlling purposes an isolated USB-serial is set up for changing gain parameters and obtain data from MCU to PC.

Chapter 5

Measurements

5.1 Piezo stack

Some measurement were done to determine dynamic behavior of the piezo stack. In Section 2.1 it is discussed about the electrical and mechanical behavior and possible mechanical resonance and anti-resonance frequencies. The electrical circuit (involving an inductor) forms a resonance circuit with capacitance of the piezo stack. If this resonance could be placed at the same frequency as the mechanical anti-resonance frequency they could cancel each other out.

First the piezo stack was measured without the inductor. Measurement was done with linear high-power operational amplifier, which was fed with signal generator. The current of the pieso was measured with a current probe. An offset voltage was introduced to the measurement signal, to prevent piezo stack from to hit any mechanical part in the test setup, where it is pushed against a chamber wall with springs. The setup is presented in Figure 5.1.

The result of the measurement is presented in Figure 5.2. Two different offset voltages were examined, however, there were now noticeable difference in graphs. The first mechanical resonance seems to be at 1.83 kHz frequency and first anti-resonance frequency at 2.1 kHz. With these results the resonance frequency could be set to anti-resonance frequency in order to cancel it out.

Capacitance of the piezo stack was measured to be 8.3 µF at 1 kHz. While the resonance frequency should be 2.1 kHz the inductance was calculate with following

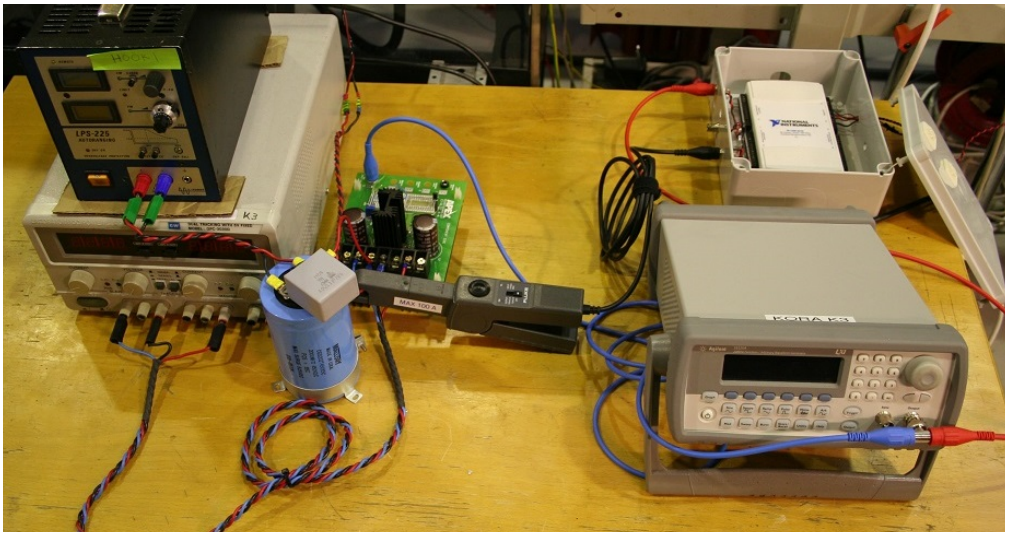

Figure 5.1: Measurement setup. Piezo stack is not shown in picture.

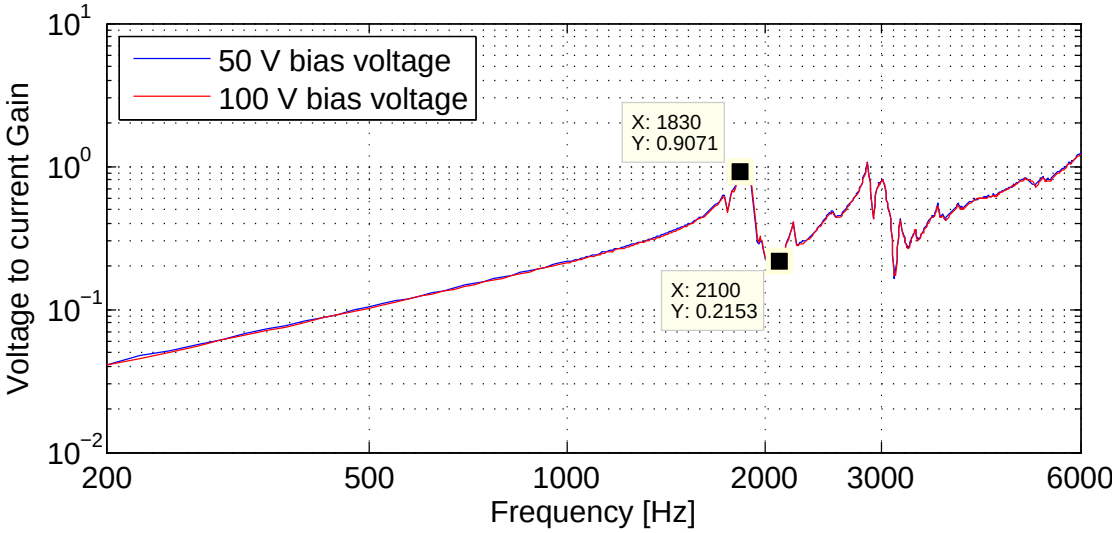

Figure 5.2: Measured piezo voltage to current amplification. Bias voltage does not seem to have any effect.

equation:

$$L = \frac{1}{(2\pi f_{res})^2 C_p}, \tag{5.1}$$

where L is needed inductance and C_p is the capacitance of the piezo stack. The result of calculation is 690 µH. A inductor was then introduced to the measurement

circuit. Three different inductance values were examined. The results are shown in Figures 5.3 and 5.4.

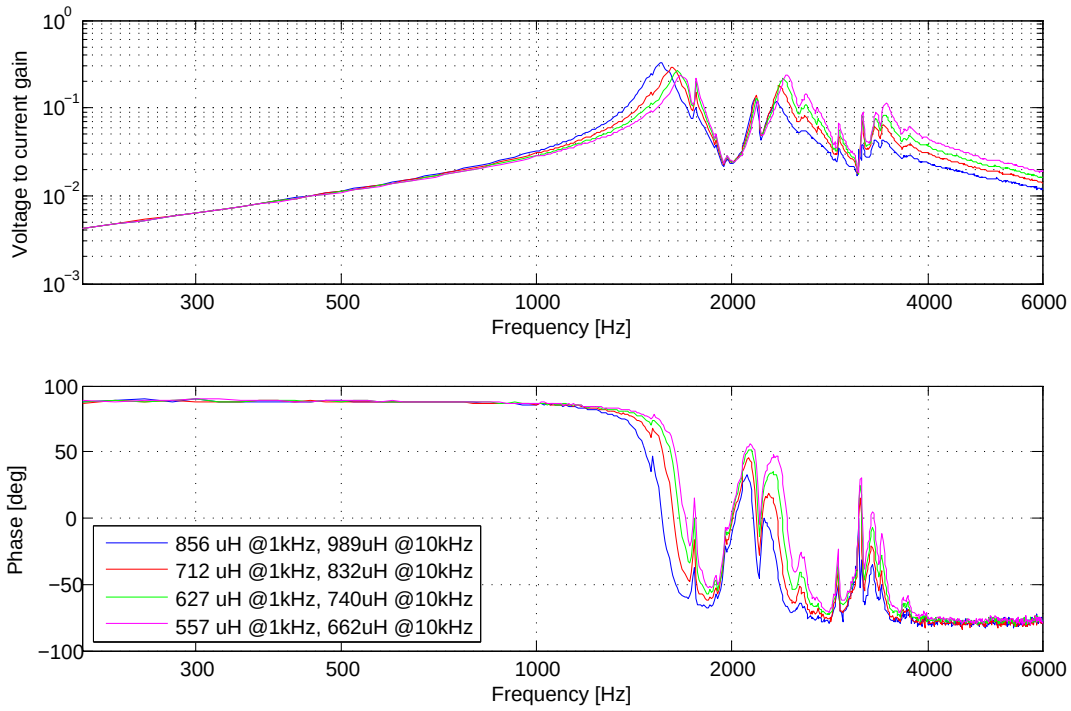

Figure 5.3: Measured piezo voltage to current amplification with four different inductance values.

The result was not quite what was expected. If Figures 2.1 and 5.3 are compared, the resonance and anti-resonance frequencies are not in same place. However, at 1.9 kHz attenuation spike is staying at same frequency. The inductance doesn't seems settle to the anti-resonance frequency. However variating the inductance seem to have effect to the first resonance spike, which varies in frequency and also in amplitude.

Also at frequencies above 3 kHz the graph seems the move according to inductance, which is expected while the corner frequency of the low-pass filter is varied.

It can be concluded that idea of placing electrical resonance frequency at the point of mechanical anti-resonance counterpart seems to be challenging. Adding a inductance to the circuit seems affects the whole frequency response instead of only one resonance peak.

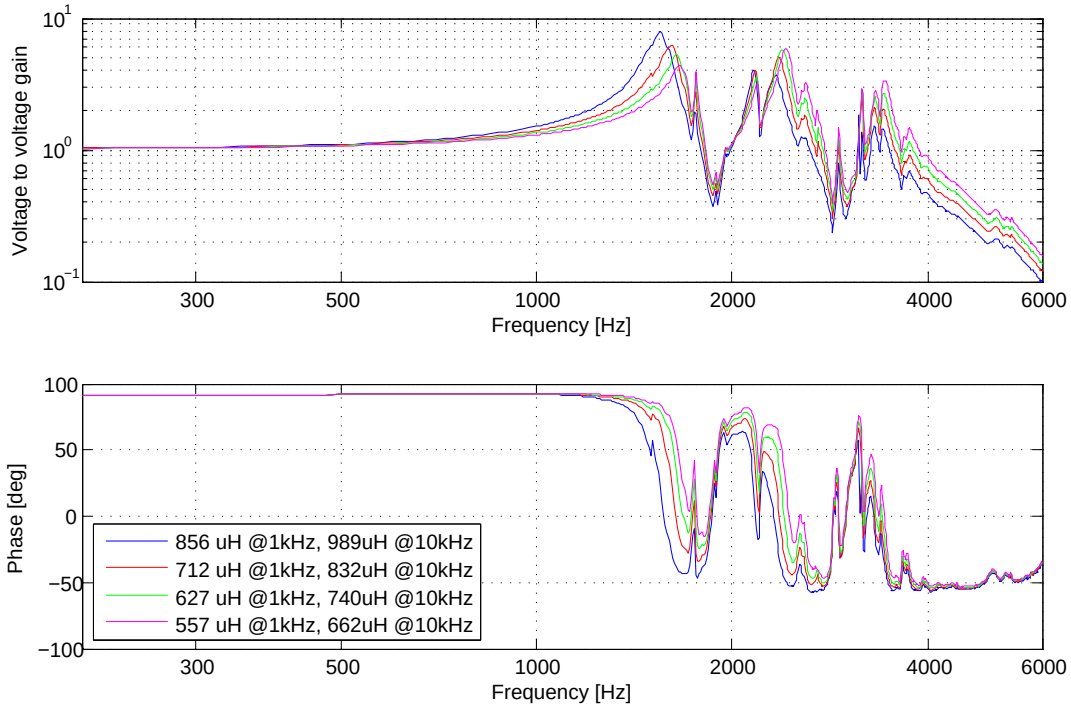

Figure 5.4: Measured piezo voltage to voltage amplification with four different inductance values.

5.2 H-bridge

At first the power supply circuit was examined and investigated, that every singal waveform is what expected. Driving a SiC MOSFET module turned out to be quite challenging. As described in Section 2.3.3 SiC technology sets many demands for the driver. The original opto-driver had to be substituted with low output impedance version. However, there was still many challenges to overcome.

Parasitic elements of the module were quite large. Especially so called Miller-capacitance causes voltage spikes in gate voltage, which can trigger unwanted shot through phenomena. Also quite small voltage margin from negative supply voltage to threshold voltage is complicating design. For example with IGBT the negative gate voltage supply can be as low as -15 V which provide almost 20 V margin before the threshold voltage. With SiC MOSFET the gate voltage cannot be driven under -5 V and the module has its own zener-diode to clamp any voltages below 5.5 V. In Figure 5.5 the gate voltage is measured while the drain-source voltage is rising during transition. There is 1 µs deadband-time between higher and lower

MOSFETs. While the higher switch turns on, a spike is formed to the gate voltage of the lower switch switch.

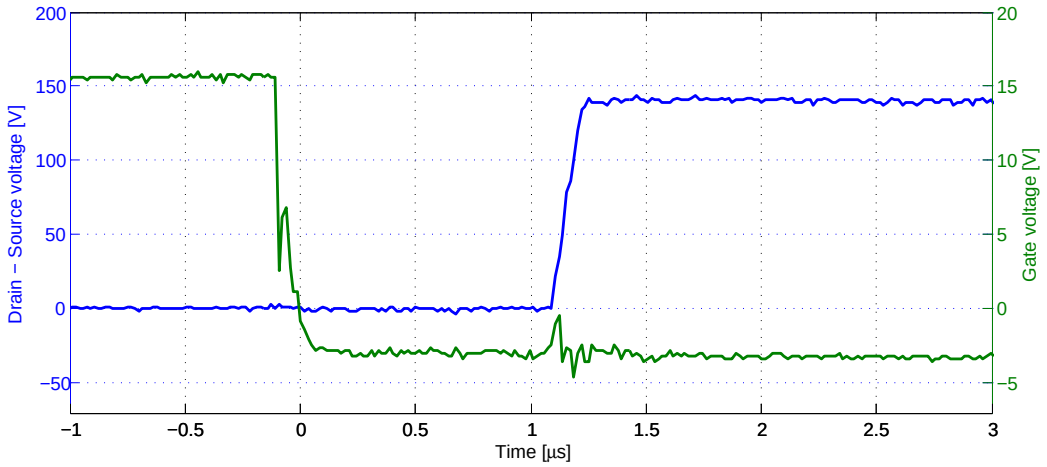

Figure 5.5: Measured piezo voltage to voltage amplification with three different inductance values.

There are few ways to overcome this problem:

- use gate driver with low output impedance and use smaller sink resistor in gate drive circuit
- increase gate capacitance with discrete component, which decreases impedance path for high frequency currents.
- use Miller -clamp circuit, which short circuits the gate node to negative rail.

The best solution would be to add a Miller clamp to the gate driver circuit, nevertheless, this requires changing the whole driver IC. Decreasing sink resistor and adding extra gate capacitance improve the situation, which can be seen in Figure 5.6.

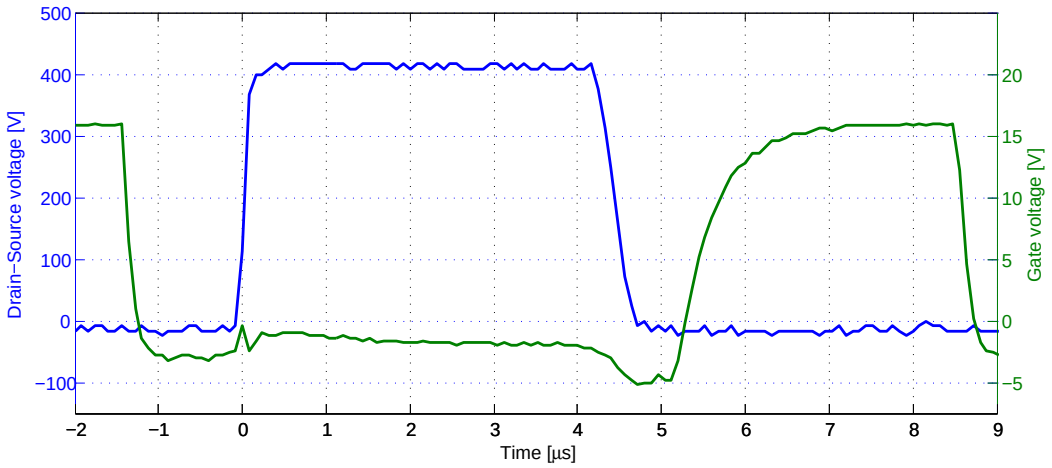

Figure 5.6: Gate voltage after adding external gate capacitance.

5.3 Driving a test load

First the topology was tested with a capacitor bank that has equivalent capacitance with the piezo stack. A biased Half-Bridge topology was used here with a unipolar switching pattern. The bias and rail voltages were 370 V an 720 V respectively while switching frequency was 50 kHz. Bias voltage was generated from a battery pack with a boost converter. Driver consumed 210W while driving waveform with 1 Hz frequency, however the warning LEDs consume approx 20 W. Also gate drivers consumed 20 W of power so the total consumption of the power supply is around 220 W. The biasing the output voltage was not taken into account because the bias capacitor is charged in discharged during rising and falling edge.

Three different voltage rise times were examined. The rising / falling edge become faster, it introduces more harmonics. As a result the resonance frequency starts to ring causing overshoot. To obtain faster response times a close loop control is needed.

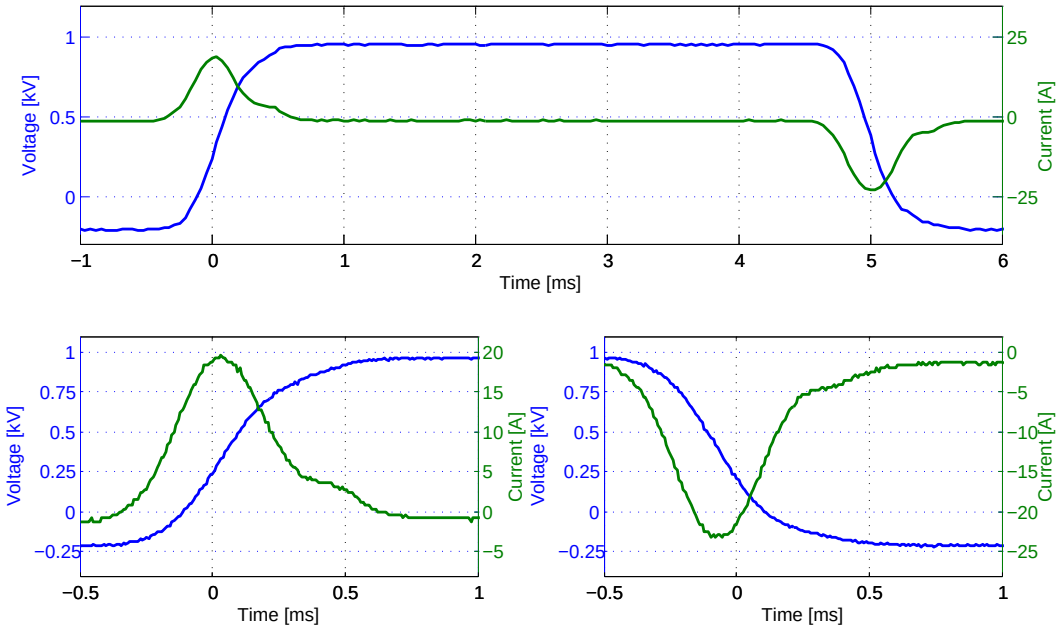

Figure 5.7: Test capacitor bank measurement with 1 ms reference rise time. Below the rising and falling edges are zoomed.

5.4 Driving piezo stack

5.4.1 Open-loop control

The power supply was attached to the piezo stack. A biased Half-Bridge topology with unipolar control was used. Bias and rail voltages were 365 V and 720 V respectively while the switching frequency was 50 kHz meaning that effectively output frequency equals 100 kHz. Also the strain of the piezo stack was captured with NAIS LM300 laser distance measurement device. In Appendix B two pictures of the test setup are shown.

The piezo stack mechanical resonances can be spotted in Figure 5.10. The strain and piezo voltage ring almost identically. Piezo voltage corresponds to strain quite well, however there is some small differences. While the voltage rises, the strain is lagging a bit. When the voltage reaches the maximum, strain is still increasing causing piezo to act as a generator when the corresponding strain is exceeded.

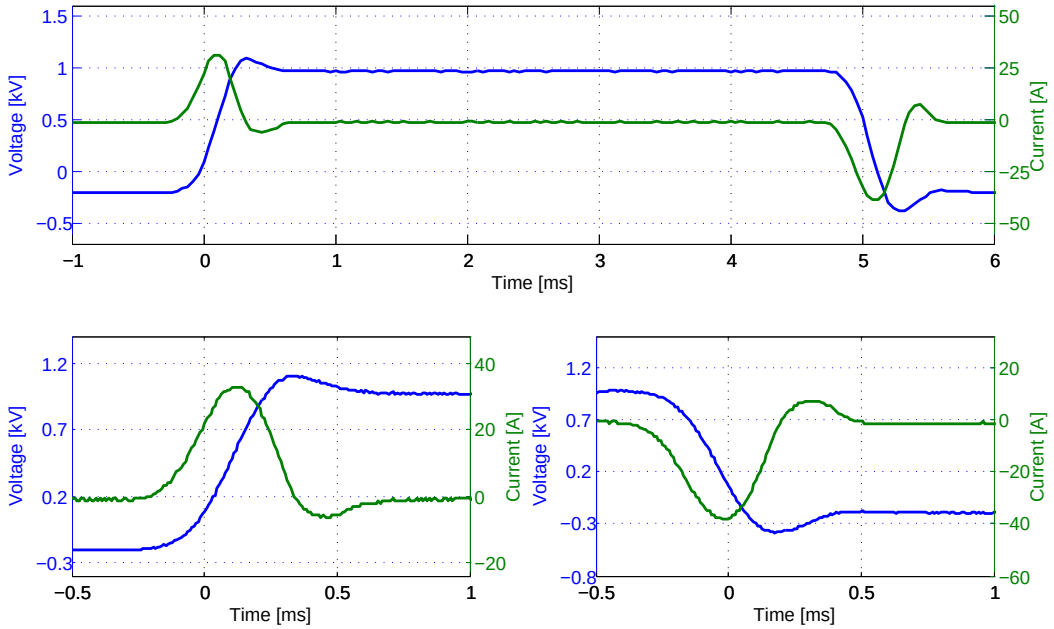

Figure 5.8: Test capacitor bank measurement with 0.75 ms reference rise time. Below the rising and falling edges are zoomed.

5.4.2 Closed-loop control

Closed-loop control was added to test behavior with voltage and current feedback. Controller block diagram is presented in Section 4.3. A Half-Bridge topology was used with bipolar switching pattern. Rail voltage and switching frequency were 150 V and 100 kHz respectively. Closed-loop control was tested with relatively low voltage compared to open-loop measurement because problems occurred with measurement circuitry.

Different shaped waveforms were tested. A lower amplitude preliminary waveform was placed before the actual one to test dynamics of the controller. Also different speed rise curves where the voltage increases with different slopes.

The controller acts quite well. There is no noticeable over or undershoot. Even more complicated waveforms are achieved with relatively simple controller.

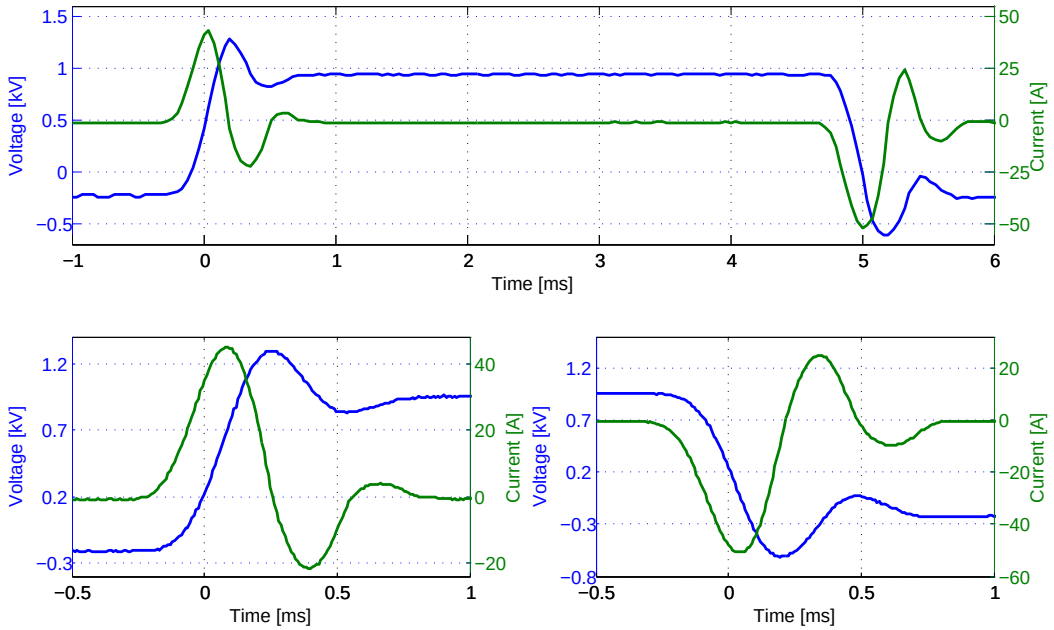

Figure 5.9: Test capacitor bank measurement with 0.5 ms reference rise time.Below the rising and falling edges are zoomed.

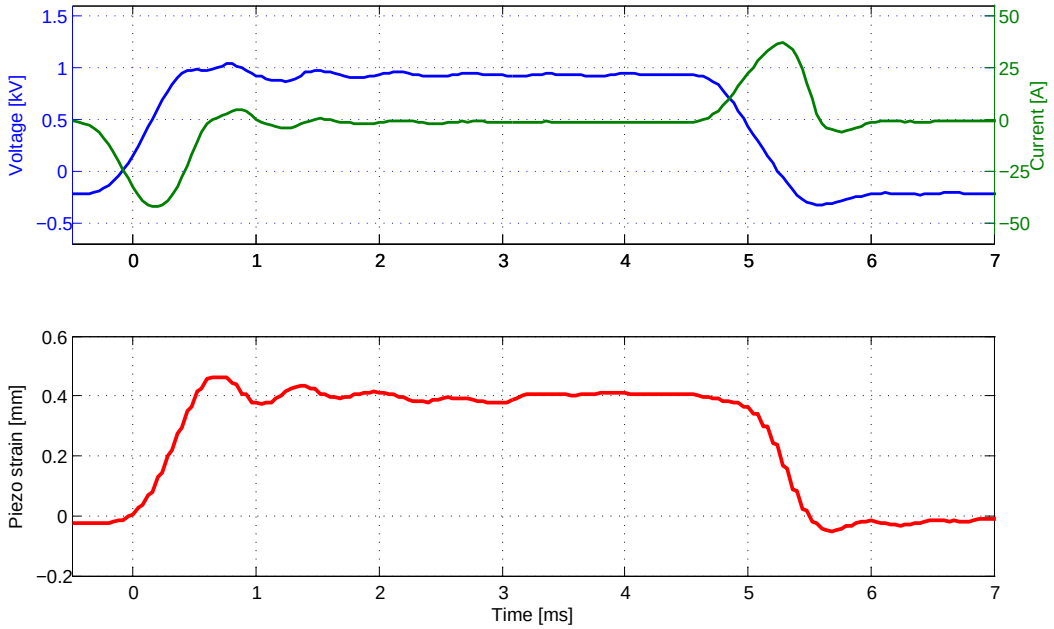

Figure 5.10: Measured voltage, current and strain of a piezo stack in open control.

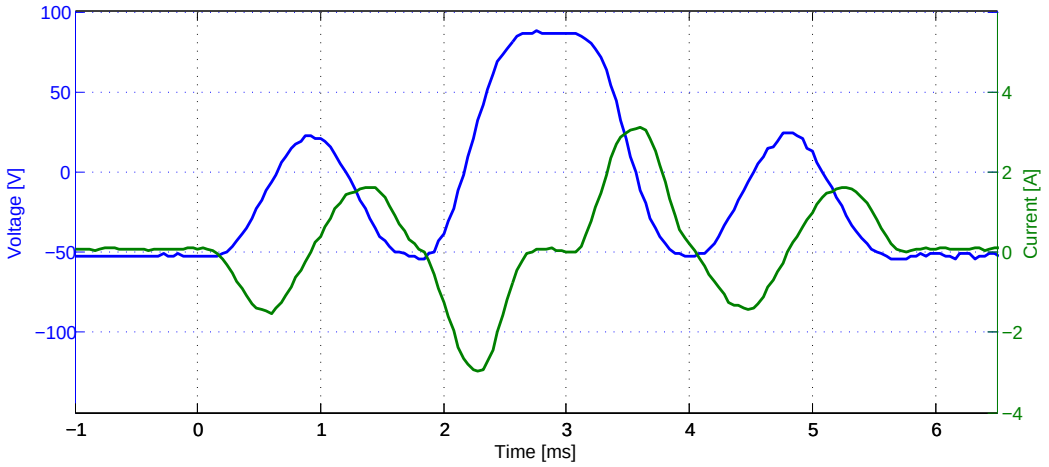

Figure 5.11: Measured voltage and current of a piezo stack in closed-loop control.

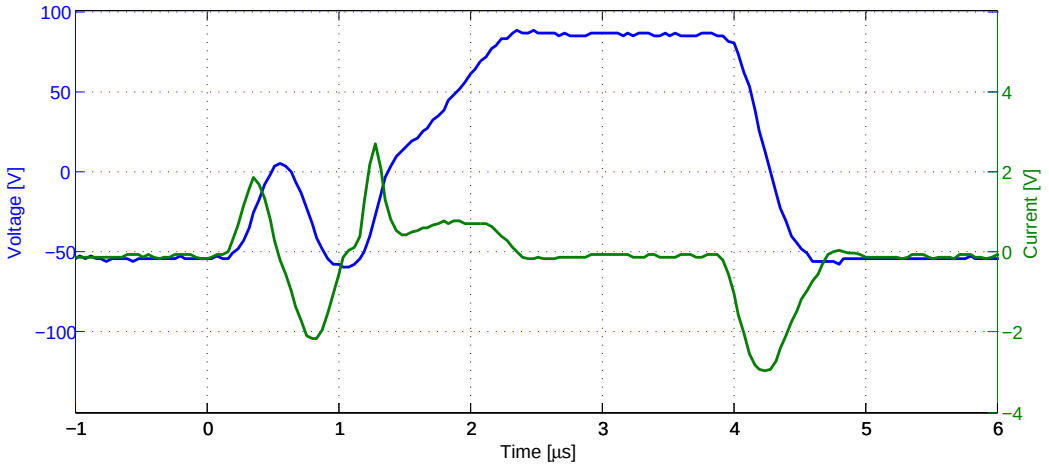

Figure 5.12: Closed loop control with variable rising slope.

Chapter 6

Conclusions

6.1 Power Supply performance

While three different concepts of the topology were simulated the biased Full-Bridge topology was actually tested with test setup. The Five-level cascaded H-bridge concept would have been also very interesting to test, unfortunately, the time run out. On the other hand the cascaded design doubles the part count of the switching devices. The biased full-bridge may be the most cost efficient topology of the simulated ones.

Generating a bias voltage is relatively easy task, nevertheless, the bypass capacitance must be quite large otherwise voltage variation may be too broad. When the piezo is charged, the bias voltage is dropped, since the load current is flowing through the bypass capacitor. If the bias voltage vary the full-bridge output voltage must compensate it in order to reach the desirable output voltage.

Bias voltage must be galvanic isolated from rest of the circuit and from ground. The capacitance between ground and bias circuit should be as low as possible while the bias setup is floating with the output voltage. Wide voltage swing in output voltage causes high currents through the capacitance.

Designed power supply could charge and discharge a high voltage piezo stack with desirable slopes. The DC-rail voltage of the full-bridge could be kept relatively low while the desirable output voltage swing could be achieved. With lower DC-rail voltage, 1200 V switching devices could be utilized. In the prototype a SiC MOSFET modules were used, though usage of IGBT is not excluded, since the

switching frequency is below 100 kHz. While the transient currents are relatively high, usage of module package is justified to avoid hot-spots from forming inside a MOSFET die. Module package is designed to have very high thermal conductivity so it can transfer heat during high current switching.

The power supply was tested with open-loop and close-loop control. Open-loop control could not produce very accurate waveforms, since the dynamics of the load is quit strict. The electrical circuit and mechanical structure of the piezo stack are forming resonances, which tend start ringing when fast transients are applied. Resonance could be damped with a resistance added across the piezo stack, which increases loses of the power supply.

Adding a current and voltage feedback along with a controller, increased the precision of the power supply. Unfortunately the controller was not been able to test with full output voltage. The controller was quite simplistic but seems to compensate the dynamics relatively well. There were no distinguishable overshoot or ringing during voltage transients.

6.2 Future improvements

Since the test equipment was designed for prototyping purposes, the size of the device was kept as big as possible in order to achieve easy access to components. If the power supply is taken into future development the size could be optimized to achieve better power-to-volume ratio.

Sic MOSFET modules used in prototype were overrated and could be optimized to cut manufacturing cost and also the volume of the device. On the other hand, used modules have very low on-state resistance and thermal resistance so they does not require heavy cooling. If the operating temperature of the device is high, the SiC MOSFET module may be justified. In future versions, gate drive circuit may need more contribution. There are demands for over voltage and over current limitations for individual valve to avoid them form destroying while undesirable condition, such as short circuit, occurs. A FPGA (Field-Programmable Gate-Array) could be utilized to achieve these limitation. Also light pipe technology could be used in order to obtain galvanic isolation between different voltage levels.

The output inductor was kept quite large in order to achieve relatively linear inductance value over wide range of output current. A high frequency iron bounder core seems to act well as the material for choke core. Saturation flux is relative high and the curve is more desirable compared to ferrite material. There is still

optimization to be made for the size and winding of the core. A litz-wire would decrease the resistance of the winding while the switching frequency is relative high and current is flowing only on the outer surface of the conductor. Introducing litz-wire were the individual strands are separated with isolated layer, decreases high frequency resistance of the winding. Also the volume of the core could be decreased when the final specifications are known.

It is also preferable to monitor the temperature of the heat sink and internal air of the power supply. Temperature may vary while the conditions outside the device change. Temperature should be kept within certain limits in order to avoid over heating. Temperature incrementation could also be a indication of a fault in the switching device or cased by a broken fan.

Measurements of piezo voltage and current could also be improved. There could be a individual current measurement for each leg of the full-bridge. If the electronics is referred to negative rail, these measurements does not need to be isolated. Thus high currents flowing during charging and discharging of the piezo, a remote voltage measurement may be better solution. This could be achieved by adding additional measurement leads besides the power leads. That way the voltage drop during current transients will not affect the voltage measurement.

There may also be demand to measure the displacement of piezo during the transition. Even though the strain of the piezo stack seems to follow the voltage well, the mechanical structure applies behavior that cannot be entirely interpreted from the voltage. There are capacitive and piezoelectric accelerometers available on market which can measure acceleration form which the displacement can be obtained by integrating twice. In the end, the movement of the piezo is the primary control value.

Adding more sophisticated controller could improve behavior of the power supply. Taking the dynamics of the piezo stack into account while designing the control should lead to very accurate results. One of the solution could a cascaded PI controller in which slower outer loop is controlling voltage. The output of the voltage controller is fed to inner current controller as reference. When the load dynamics are well known a Model Predictive Controller (MPC) could be used. MPC could predict the behavior of the output in near future with help of the load model. MPC also takes the system limitations into account and is easy to tune. [33]

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Appendix A

Prototype pictures

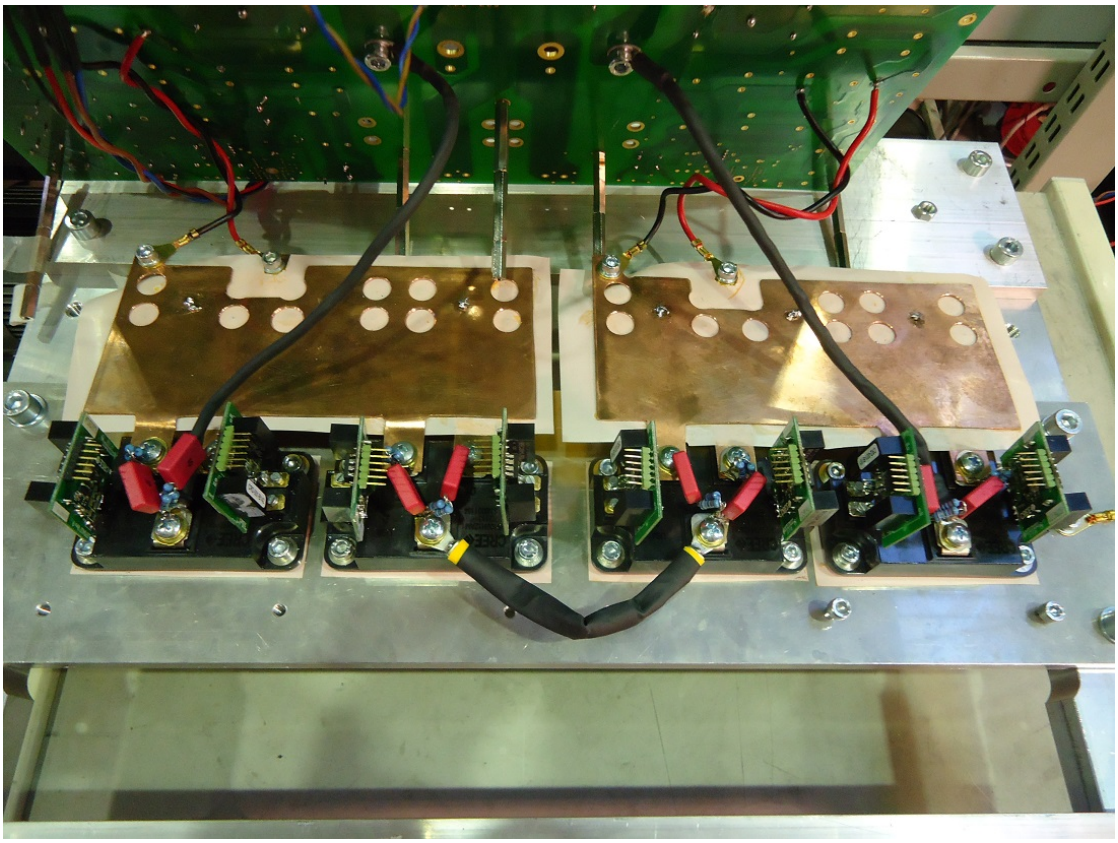


Figure A.1: Picture fo the DC rails and SiC MOSFET module with gate driver circuits attached.

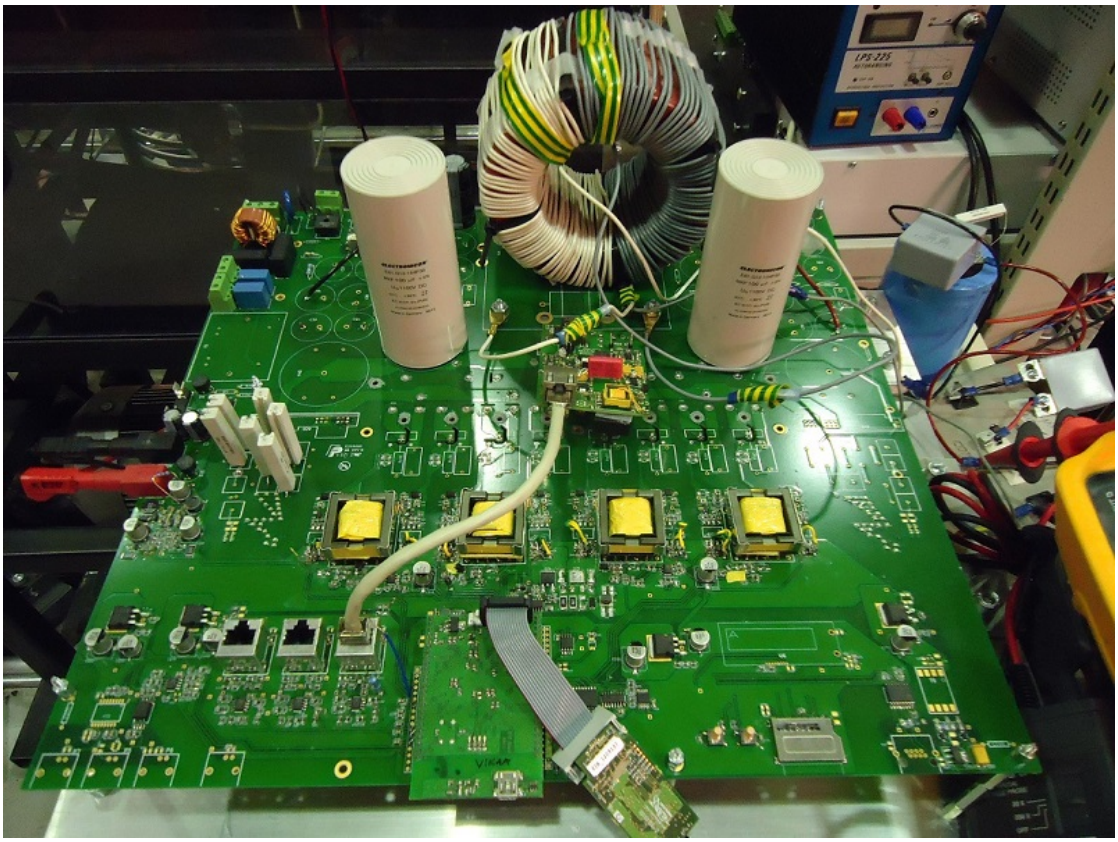


Figure A.2: Picture of the main printed circuit board. The output inductor is placed on top of the board. A JTAG programming is attaced to the Microcontroller daughter board. A measurement daughter board is attached with a wire.

Appendix B

Test setup

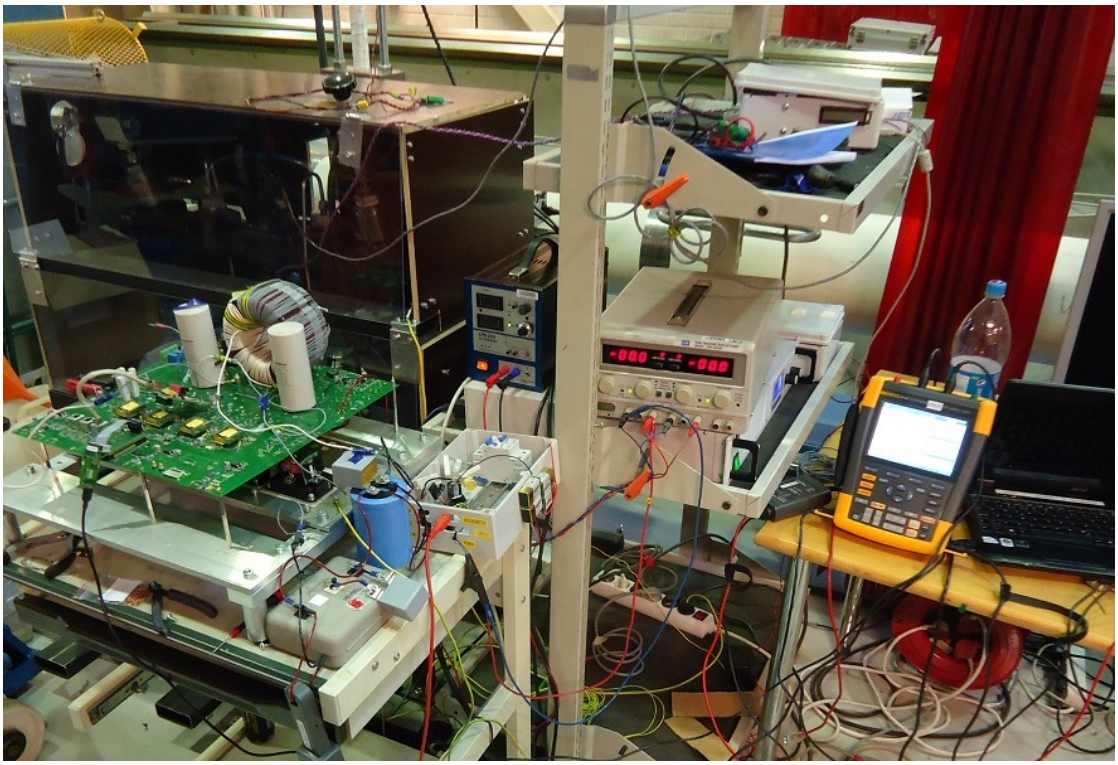
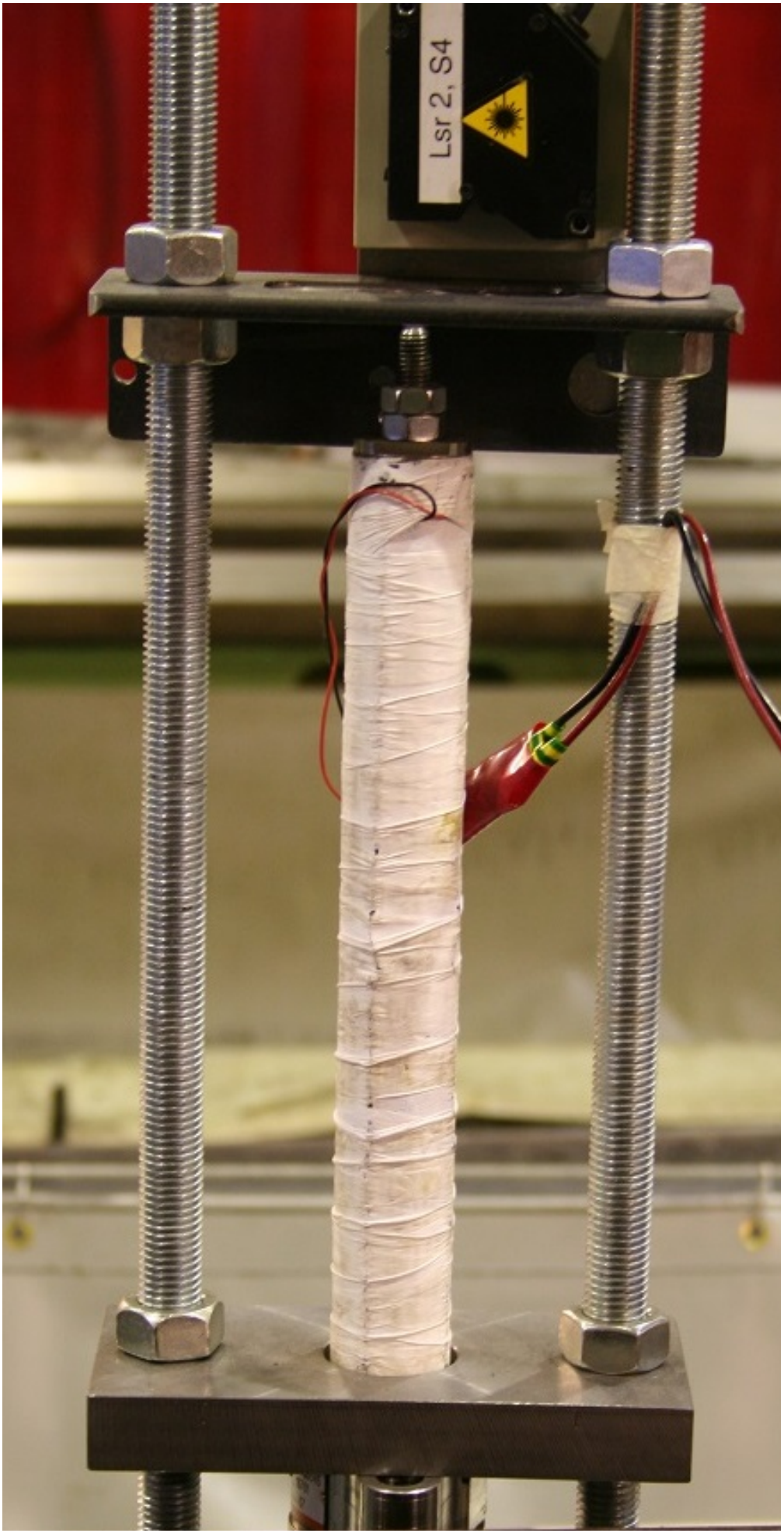


Figure B.1: Testing setup of the piezo driver.


Lsr 2, S4